

Integrated, Multichannel Readout Circuit Based on Chopper Amplifier Concept for FET-Based THz Detectors

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Abstract This work presents the integrated, multichannel readout circuit dedicated to FET-based THz detectors. Described solution provides an unique approach to FET detectors readout, able to replace the measurement equipment deploying the lock-in technique and to eliminate the necessity of modulating the THz wave. The IC proposed by the authors is based on the chopper amplifier architecture, enhanced and adapted for multichannel signal processing. It also ensures significant $1/f$ noise minimisation, which is the key requirement for the FET-based detectors readout. The circuit prototypes were manufactured in standard 350 nm CMOS process (AMS A.G.) and then measured in the dedicated test set-up.

Keywords Readout circuit · FET-based THz detector · Chopper stabilisation · Gm-C filter · Phase-sensitive detection (PSD)

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1 Introduction

When illuminated by THz radiation, the nonlinear properties of a field effect transistor (FET) lead to the photovoltaic effect, resulting in a very small DC voltage (usually up to tens of μV) measured between its source and drain electrodes. The detection mechanism occurs for the frequency range that is appreciably higher than the device cut-off frequency—this fact enables the manufacturing of detecting transistors in not expensive, legacy silicon processes. The first experimentally proven (sub)terahertz detection by FET was reported by Lu in 1998 [22] (using high electron mobility transistor—HEMT). During the next several years, many studies have been reported demonstrating detection of THz radiation in commercial AlGaAs/GaAs FET [13], double quantum well FET with a periodic grating gate [27], AlGaN/GaN HFET [15], Si MOSFET [16] and junctionless FET [23]. Nowadays, FETs are considered to be one of the most promising solutions dealing with the detection of THz radiation. These devices ensure low fabrication costs, satisfactory parameters achieved at room temperature and easy on-chip integration with a readout electronics [14,33]. Over the last few years, many studies have been reported (e.g. [3,20,28,30]) concerning development of FET-based THz imaging arrays.

The systematically rising significance of the FET-based THz detectors stimulates the research work aimed at the readout circuits addressed to these devices. Nowadays, most of experimental studies concerning deployment of FETs for THz applications are performed using the lock-in technique (in general phase-sensitive detection—PSD). In this method the useful signal is extracted from the background noise and other interferences by its modulation with some reference frequency and phase. With undisputed advantages of the lock-in technique, this method is also limited by some fundamental restrictions: measurements are relatively slow, some THz sources cannot be easily modulated (e.g. the natural background THz radiation), it requires permanent synchronisation between the modulated signal source and the measurement circuit. Also the standard lock-in apparatus is usually a heavy (often rack-mounted) device equipped with a dedicated preamplifier to limit parasitic RC parameters.

In the vast majority of studies, published within the last several years and dealing with the FET-based detectors measurements and their potential applications, the lock-in amplifier is used as an essential component of test set-up and is required for proper readout operation (a few representative examples can be found in [4,25,32]). This also concerns imaging systems mentioned before (THz imagers described in [20] and [30]), where the use of lock-in amplifier is in total contradiction with target mobility and universality of developed devices. There are limited solutions (for example the THz video camera reported in 2012 [10]) which do not require PSD, but they usually come down to a very simple readout electronics integrated with the detector (in [10] it was just a transistor differential pair) and complicated, externally amplifier unit consisted of several off-the-shelf components.

There is also a possibility to analyse the output current of FET-based detectors instead of voltage, e.g. [7]—it seems promising from a potential signal-to-noise ratio point of view. Nonetheless, this paper is focused on the voltage-mode processing.

In this work, the authors present the new integrated readout circuit intended to operate with FET-based THz detectors. It has been experimentally proven that proposed

IC can successfully replace the lock-in equipment offering comparable parameters but without the necessity of modulating the THz wave and using complex and expensive measurement equipment. Described solution provides new possibilities in the field of FET detectors and readout electronics integration, resulting in miniaturisation of the THz imaging or spectroscopy systems.

2 Chopper Stabilisation

The proposed readout solution is based on the well-known chopper stabilisation technique. According to [36], this approach was first introduced in 1948 by Goldberg and to this day a great progress has been made in these amplifiers characteristics. In general, chopper amplifier modulates the input DC voltage with reference frequency f_{chop} , amplifies this AC signal, and then synchronous demodulation is provided to restore the DC signal. This approach minimises the input offset voltage and $1/f$ noise impacts, because only an AC component is selectively amplified. Overall principle of this operation is illustrated in Fig. 1.

Waves $m_1(t)$ and $m_2(t)$ are the modulating and demodulating signals of $T = \frac{1}{f_{chop}}$ period (we assume 50% duty cycle), V_{OS} and V_N stand for deterministic DC offset and noise. To avoid the potential signal aliasing, it is also assumed that the input signal frequency is limited to half of the f_{chop} .

As it is shown in Fig. 1, the modulation process transposes the input signal to the odd harmonic frequencies of the $m_1(t)$. After selective amplification, the signal is then demodulated by multiplying $m_2(t)$ —this operation moves processed signal to the even harmonics of $m_2(t)$. The ideal, noiseless output contains significant DC component of a value corresponding to the input signal and several others, higher frequency components concentrated around mentioned even harmonics. To recover the original amplified signal, $V_{out}(t)$ has to be applied to a low-pass filter with a cut-off frequency slightly above the input signal bandwidth.

In the practical case, the amplifier applied in the circuit introduces the offset voltage V_{OS} and noise component V_N , but they are modulated only once (by $m_2(t)$) and

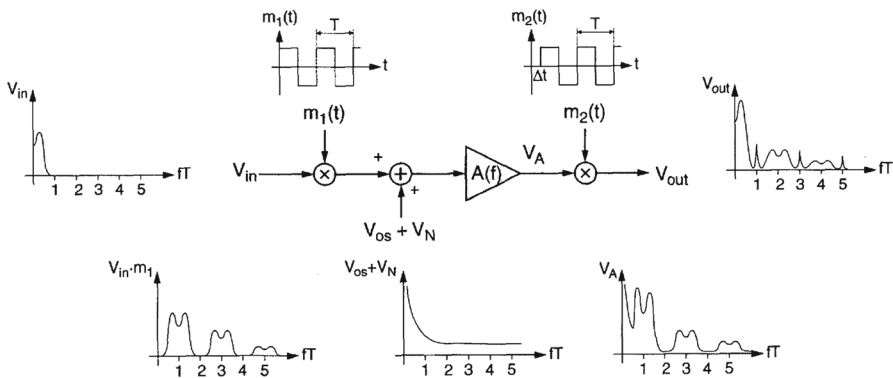


Fig. 1 Chopper stabilisation principle [8]

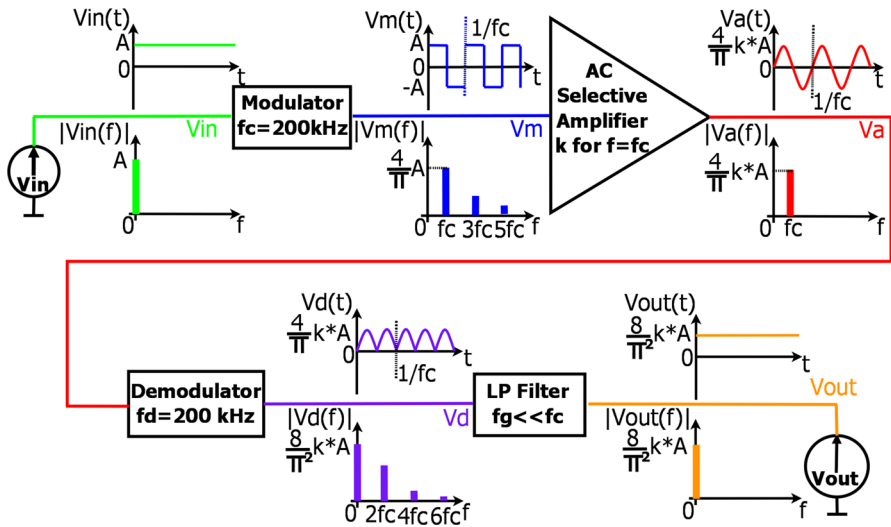


Fig. 2 Simplified chopper amplifier principle

transposed to the odd harmonics of the demodulating signal. Then they can be easily filtered out, leaving the amplifier without any offset neither the low-frequency noise.

In case of the FET-based detectors readout circuit, the input signal is a pure DC voltage (when ignoring at this point the thermal noise of the transistor channel). This results in the simplification of the signal processing analysis presented above. Figure 2 shows the chopper amplifier architecture overview for an input DC signal, with ideally selective and noiseless AC amplifier and with a low-pass filter placed at the end of the signal path.

With these assumptions, modulated signal is just a square wave of the amplitude equal to the input signal amplitude (marked as k according to the symbols presented in Fig. 2). The trigonometric Fourier series expansion of this signal is given by the Eq. (1):

$$V_m = \frac{4k}{\pi} \sum_{n=1,3,5\dots}^{\infty} \frac{\sin(n\omega_{chop}t)}{n} \tag{1}$$

Selective amplification results in a sine wave of the amplitude $\frac{4}{\pi} \cdot k \cdot A$, and the demodulation process provides a rectification of this signal, producing (2):

$$V_{out}(t) = \frac{8 \cdot k \cdot A}{\pi^2} - \frac{16 \cdot k \cdot A}{\pi^2} \sum_{n=2,4,6\dots}^{\infty} \frac{\cos(n\omega_{chop}t)}{(n^2 - 1)} \tag{2}$$

The output LP filter suppresses all higher frequency components, which causes final output signal to be a pure DC of $\frac{8 \cdot k \cdot A}{\pi^2} \approx 0.81$ kA amplitude.

The delay introduced by the AC amplifier can result in a degradation of the chopper amplifier gain calculated above. For example, if the AC amplifier produces a constant delay of $\frac{T_{chop}}{4}$ while the modulator and demodulator circuits are in phase, the output

signal will be chopped in cosinusoidal way resulting in no DC component and only odd harmonics. In this case, the overall DC gain of the chopper stabilised amplifier is zero. This extreme example shows that in order to maintain a maximum DC gain, the phase shift between the modulator and the demodulator has to match precisely the phase shift introduced by the amplifier.

3 Multichannel Readout IC

3.1 Basic Principles

Basing on the chopper stabilisation technique described above, the integrated readout circuit dedicated to the FET-based THz detectors has been designed. The small voltage generated over the relatively high output impedance of a FET device operating in the sub-threshold region has required the high gain and high input impedance of the readout circuit, while the DC nature of this response made it necessary to pay the special attention to the $1/f$ noise components. At the same time, designed readout IC was intended to replace the lock-in equipment and to eliminate the need of a THz wave modulation. The circuit also had to provide multichannel signal processing, supporting readout of detector lines or arrays. The designed IC provides the readout circuit functionality for eight-element pixel-line of FET-based THz detectors, but it can be easily adopted to build the larger, more complex system. Figure 3 presents the overall view of proposed integrated circuit.

As it is shown, the signal path can be divided into two different parts: individual channels for each particular detector and the common signal processing path. The main idea behind this semi-parallel structure was to reduce the area of designed chip, the number of required pads, and to provide common analog output, easy to handle by a single-channel ADC. The signals from eight detectors are independently modulated, amplified and filtered by bandpass Gm-C amplifiers. Then internal multiplexer selects which pixel is currently connected to the common part of the signal path, providing second stage of selective amplification (using multiple feedback topology (MFB) filter), demodulation and low-pass filtration (by second-order Sallen–Key filter). Each Gm-C amplifier provides gain of $100 \frac{\pi^2}{8} [V/V]$ (for f_{chop}), and MFB filter ensures $-10/-100 [V/V]$ (set by 1-bit control signal), which results in total gain of 60/80 [dB]

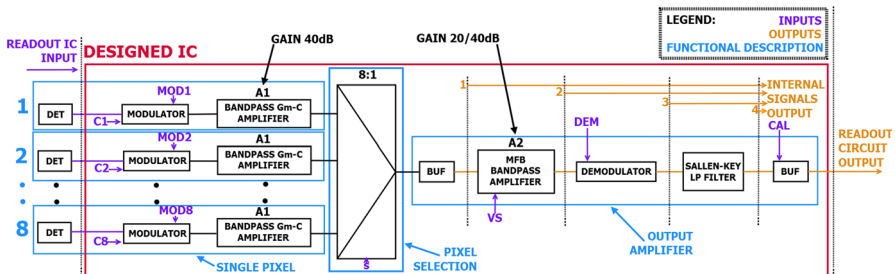


Fig. 3 Architecture of designed readout circuit

with inverted signal phase. These values are sufficient to provide the satisfactory signal processing for FET-based THz detectors. This has been experimentally confirmed by the authors and is strictly related to the detectors sensitivity and output power of applied THz source (results presented in this paper have been obtained using the VDI, Inc. 340 GHz transmitter with 2 mW of total power).

The system partitioning between individual and common parts of the signal path described above has been chosen during the analysis of several positions of potential split point. Simple switching of a detectors to one, common single-pixel readout circuit is impractical due to the distortions introduced by a switching process, dominating the very low output signal produced within the detector. Another reason is relatively large time constant of effective output impedance of detecting FET (several hundreds of $k\Omega$) and input capacitance of the readout circuit, resulting in a very low switching frequency obtainable. In proposed solution, the split point is introduced just after the first gain stage succeeding the modulator. In this case, the signal amplitude is sufficient to consider the switching distortions as negligible.

Proposed architecture can be used in many imaging applications, where the speed of system operation is not a critical parameter, and individual pixels can be read sequentially. To provide the readout electronics for detector lines/arrays containing more than eight elements, several ICs can be combined together using external multiplexing. In case when the higher processing speed is desired, the circuit can be also easily redesigned to a fully parallel structure enabling simultaneous access to all channels, at the expense of the area cost, power consumption and number of pads required.

The system provides differential signal processing together with the ability of the input and output offset compensation. Each channel is equipped with differential inputs: the positive one is intended to handle the detector, while the second one (C1...C8 in Fig. 3) can be driven by an offset compensation network, controlled externally. The output buffer also provides the DC offset compensation by means of the appropriate control signal (CAL in Fig. 3).

3.2 Modulator and Demodulator Circuits

The modulator and demodulator are designed as switching circuits, each of them is composed of four pairs of CMOS switches. Their scheme is shown in Fig. 4a—it is a typical architecture used in chopper amplifiers, presented for example by Enz et al. in [9].

Both DC input voltages are fed alternately to the positive and negative output pins, resulting in a differential output square wave, of a frequency equal to the chopping frequency of the entire readout amplifier. In this work, the 200 kHz has been chosen as a trade-off between manufacturing process restrictions (AMS C35) and the low-frequency ($1/f$) noise minimisation requirement.

The channel capacitance of a switching transistors causes unwanted charge injection phenomenon, resulting in voltage spikes at the output of modulator and demodulator circuits. During the switching-off process, an electric charge stored in the transistor channel exits through its source and drain terminals (leakage to the bulk electrode can be ignored). The precise relation between the amount of charge flowing to the source

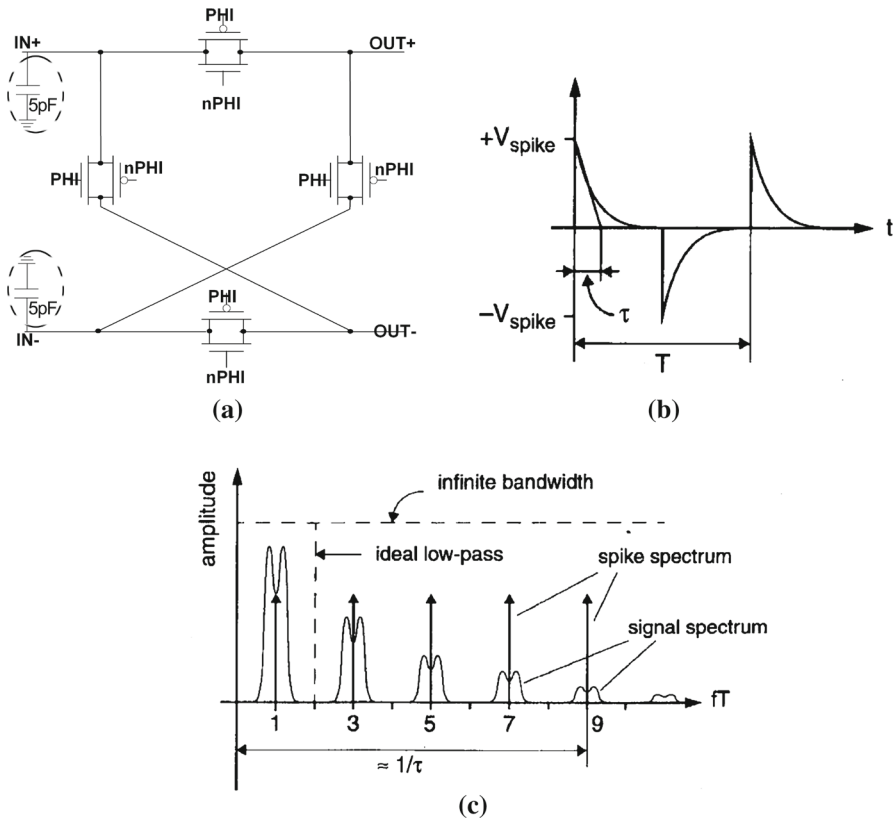


Fig. 4 Modulator and demodulator details: **a** circuit architecture, **b** voltage spikes caused by the charge injection phenomenon [36] and **c** spectrum of the voltage spikes and modulated input signal [9]

and drain is related to the ratio of total capacitance connected to these terminals, to the transistor on-resistance and the slope of the clock signal applied to the gate [36]. In general, the larger the source or drain capacitance is (with respect to the other one), the bigger amount of charge flows to this electrode.

The charge injection causes voltage spikes that appear at the AC amplifier input (Fig. 4b) and can be amplified and demodulated resulting in residual DC offset at the circuit output. Assuming that a half of the charge stored in the channel is injected to the drain area, the amplitude of a single spike generated by a turning off transistor can be evaluated by the Eq. (3) [29]:

$$V_{\text{spike}} = \frac{WLC_{\text{ox}}(V_{\text{DD}} - V_{\text{in}} - V_{\text{th}})}{2C_D}, \tag{3}$$

where W and L denote channel width and effective length, C_{ox} is gate oxide capacitance per unit area, C_D total drain capacitance, V_{DD} corresponds to voltage amplitude of switching control signal, V_{in} for input voltage and V_{th} for threshold voltage.

The pulse width of the spikes (τ in Fig. 4b, c) is in general much smaller than the period of the chopping signal, so most of their energies are concentrated at frequencies higher than the chopping frequency. Using an AC amplifier of a bandwidth limited slightly above than the f_{chop} , most of the residual offset is filtered out. Assuming the AC amplifier bandwidth equal to the doubled chopping frequency, the input-referred voltage offset produced by the switch charge injection can be described as [9]:

$$V_{\text{OS}} \simeq \left(\frac{2\tau}{T}\right)^2 V_{\text{spike}} \quad (4)$$

In the proposed chopper amplifier circuit, several techniques dealing with the reduction in the charge injection effect have been used. Firstly, each transistor switch is composed of two complementary FETs, NMOS and PMOS, connected in parallel (see Fig. 4a). In an ideal situation, charge injected by these two devices cancel each other—this can be achieved only when $W_{\text{NMOS}}L_{\text{NMOS}}C_{\text{ox}}(V_{\text{DD}} - V_{\text{in}} - V_{\text{thn}}) = W_{\text{PMOS}}L_{\text{PMOS}}C_{\text{ox}}(V_{\text{in}} - |V_{\text{thp}}|)$. As it is shown, perfect compensation occurs only for a specific value of the input voltage. Fortunately, in case of processing the signals produced by FET-based THz detector, it can be assumed that this input voltage is constant and nearly equal to zero (the actual values usually will not exceed tens of μV).

Secondly, a fully differential structure of the modulator/demodulator has been used (see Fig. 4a). If the amounts of charge injected by two complementary switches are matched, the resulting voltage appears as a common mode voltage and therefore it is rejected.

Thirdly, internal 5 pF capacitors have been connected in parallel to each modulator input (marked with dashed outline in Fig. 4a), decreasing the amount of charge injected to the AC amplifier input—by increasing the ratio between input and output capacitances of the switch. Naturally, this limits the processing speed of the designed chopper amplifier, but—as it was already mentioned—in this particular case that is not a key parameter. Also it is worth to be pointed out that the dominating speed restriction is enforced by the output LP filter characteristic (see schematic in Fig. 3).

3.3 Bandpass Gm-C Amplifier

According to the architecture presented in Fig. 3, first-stage amplification of the processed signal is carried out by the Gm-C amplifiers. The designed bandpass biquad section bases on the well-known concept, summed up by Tsvividis in [35]. The overall structure is shown in Fig. 5.

The transconductor g_{m1} controls the gyrator circuit, C capacitance and transconductor g_{m2} by converting the input voltage into current and feeding the input to the biquad section. This circuit models an LCR filter with g_{m2} performing a role of a resistor and controlling the pole-Q of the filter. The aforementioned gyrator is composed of the transconductors g_{m3} and g_{m4} loaded by the C_L capacitor. Under these conditions, the gyrator transforms C_L capacitance into L_Z inductance, according to the Eq. (5):

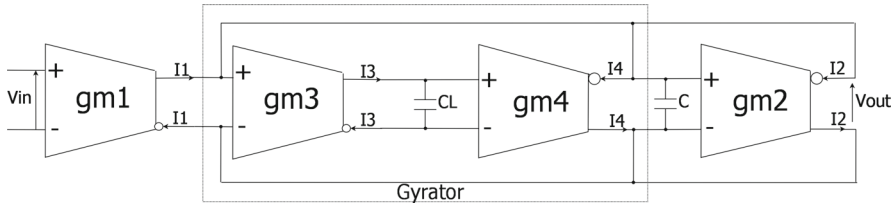


Fig. 5 Designed bandpass Gm-C amplifier

$$L_Z = \frac{C_L}{g_{m3} \cdot g_{m4}} \tag{5}$$

This solution is called the floating gyrator-C inductor and has been introduced in late 60s by Holmes et al. in [11]. The gyrator together with the C capacitance forms an LC resonant circuit. The overall Gm-C filter transfer function can be described by the Eq. (6):

$$\frac{V_{out}}{V_{in}}(s) = \frac{\frac{g_{m1}}{C} s}{s^2 + s \frac{g_{m2}}{C} + \frac{g_{m3} \cdot g_{m4}}{C_L \cdot C}} \tag{6}$$

This leads us to the main parameters of the presented biquad section (Eqs. 7–9).

$$\omega_0 = \sqrt{\frac{g_{m3} \cdot g_{m4}}{C_L \cdot C}} \tag{7}$$

$$Q = \frac{\sqrt{g_{m3} \cdot g_{m4}}}{g_{m2}} \cdot \sqrt{\frac{C}{C_L}} \tag{8}$$

$$k(\omega = \omega_0) = \frac{g_{m1}}{g_{m2}} \tag{9}$$

In the formulas presented above ω_0 denotes the resonant pulsation, Q is the filter quality factor and k corresponds to the circuit gain for the resonant frequency.

As it is shown, the parameters described above are defined by the transconductance of deployed g_m -cells. It is extremely important to keep this transconductance constant for the wide range of processing voltage amplitudes, providing the stability of the main biquad section parameters. For that reason, the transconductor linearisation technique using source degeneration has been used (introduced and described in [17]).

Figure 6a presents a differential pair with the source degeneration using MOS transistors.

Starting with the basic MOSFET I–V equations, the formula for the differential transconductance of a simple differential pair can be calculated as (Eq. 10):

$$G_{mr} = \frac{\partial I_d}{\partial V_i} = \frac{2K_{1,2}}{\sqrt{\frac{2I_S}{K_{1,2}} - V_i^2}} \left(\frac{I_S}{K_{1,2}} - V_i^2 \right), \tag{10}$$

where I_i, V_i are differential output current and differential input voltage, $K_{1,2} = \frac{1}{2} \mu_n C_{ox} \frac{W_{1,2}}{L_{1,2}}$ and I_S denotes biasing current.

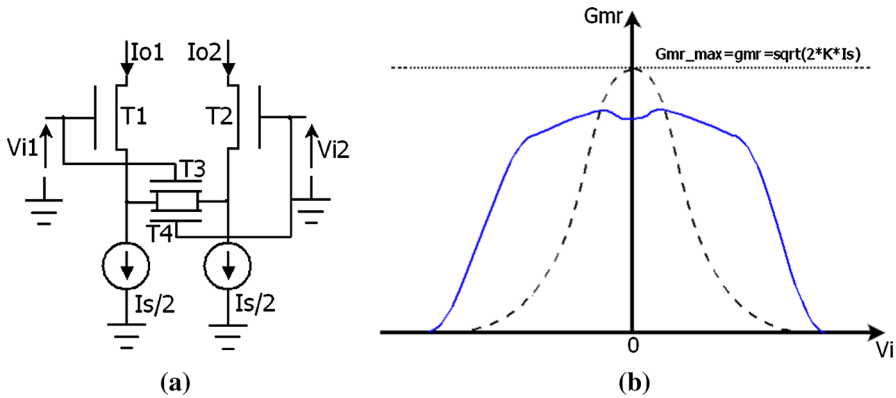


Fig. 6 Transconductor linearisation technique using source degeneration: **a** differential pair with source degeneration using MOS transistors (based on the concept presented in [17]) and **b** differential transconductance of simple differential pair (*dashed*) and differential pair with source degeneration (*solid*)

The exemplary transconductance curve as a function of input voltage is presented in Fig. 6b. The transconductance linearity can be improved by adding two parallel transistors, connected in-between the input transistors sources—as it is shown in Fig. 6a. The transconductances of T3 and T4 are placed in series with respect to the T1 and T2 transconductances. These degeneration transistors form a specific resistor controlled by the input voltage. Both of them operate in a triode region and implement dynamic linearisation of circuit I–V characteristic: when differential input voltage increases, transconductances of T1 and T2 decrease, but it is compensated by the drop of r_{ds} of T3 and T4. Linearised differential transconductance of the entire circuit is described by Eq. (11):

$$G_{mr} = \frac{2K_{1,2}}{\alpha \sqrt{\frac{I_S}{K_{1,2}} - \frac{8U_i^2}{\alpha^2}}} \left(\frac{I_S}{2K_{1,2}} - \frac{8U_i^2}{\alpha^2} \right), \tag{11}$$

where $\alpha = 1 + \frac{K_{1,2}}{4K_{3,4}}$ and remaining symbols are identical as used in Eq. (10). The linearised transconductance curve is illustrated in Fig. 6b.

Figure 7 presents the architecture of designed transconductors cell. It is based on the fully balanced transconductor amplifier presented in [17], expanded by the additional common mode feedback (CMFB) circuit. T1–4 form the differential pair with source degeneration described above, with T5–6 operating as the active load. T7–T9 compose current mirror biased by T10, while T11–T18 form a CMFB block, controlling the common mode voltage at circuit outputs by introducing the negative feedback (setting the gate bias of T5–6 accordingly to the differential output voltage).

All designed transconductors cells, previously shown in Fig. 5, have almost identical schematic, differing only in transistor dimensions, which results in different transconductance values. For input signals up to 100 mV, $g_{m1} = 520 \mu\text{S}$, $g_{m2} = 46.8 \mu\text{S}$, $g_{m3} = g_{m4} = 10 \mu\text{S}$ and $C_L = 6.3 \text{ pF}$, $C = 10 \text{ pF}$. According to the Eqs. (7)–(9), these values determine the main circuit parameters as $\omega_0 \simeq 2\pi 200 \text{ kHz}$, $Q \simeq 0.34$, $k(\omega = \omega_0) \simeq 10 \frac{\pi}{2\sqrt{2}} \simeq 11.11$. The total gain for $f_0 = 200 \text{ kHz}$ of each Gm-C

In general both filter topologies are based on the well-known circuit solutions: multiple feedback bandpass filter (MFB) and second-order Sallen–Key low-pass filter. These architectures have been described in many text books and journal papers, e.g. in [18].

The selective amplification is ensured by the second-order filter, presented in Fig. 8a. Its transfer function is given by the Eq. (12), and its main parameters are described by the Eqs. (13)–(16):

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = \frac{-sC \frac{R_2 R_3}{R_1 + R_3}}{1 + sC \frac{2R_1 R_3}{R_1 + R_3} + s^2 C^2 \frac{R_1 R_2 R_3}{R_1 + R_3}} \quad (12)$$

$$\omega_0 = \frac{1}{C} \sqrt{\frac{R_1 + R_3}{R_1 R_2 R_3}} \quad (13)$$

$$Q = \frac{\omega_0 R_2 C}{2} \quad (14)$$

$$\text{Bandwidth} = \frac{1}{\pi R_2 C} \quad (15)$$

$$k(\omega = \omega_0) = -\frac{R_2}{2R_1} \quad (16)$$

For the sake of compatibility with the wide range of FET-based THz detectors, the developed readout circuit ought to provide the gain control. For that reason, the authors decided to use the selective filter based on the multiple feedback topology instead of the Gm-C filter (described in Sect. 3.3), because the MFB architecture allows to adjust the gain with constant resonant frequency and quality factor. In the designed chip, R_1 is used to alter the gain value (see Eq. 16), while the resonant pulsation (13) can be kept constant by simultaneous change of the R_3 , resulting in constant quality factor and bandwidth (14 and 15). Presented solution set $R_1 = 4.2 \text{ k}\Omega/42 \text{ k}\Omega$, $R_2 = 840 \text{ k}\Omega$, $R_3 = 17 \text{ k}\Omega/3.65 \text{ k}\Omega$, $C = 15 \text{ pF}$, resulting in $k(\omega = \omega_0) = -100/-10 [V/V]$, $\omega_0 = 2\pi 200 \text{ kHz}$, $Q = 8.8$.

The designed output LP filter is based on unity-gain Sallen–Key architecture, presented in Fig. 8b. This circuit is characterised by the cut-off frequency significantly lower than the chopping frequency $f_c = 200 \text{ kHz}$, and its role is to convert the rectified sine wave into a DC signal (see Fig. 3). The transfer function of applied LP filter is given by Eq. (17), and its cut-off frequency is described by (18).

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = \frac{1}{s^2 + \frac{2s}{RC} + \frac{1}{R^2 C^2}} \quad (17)$$

$$f_c = \frac{1}{2\pi RC} \quad (18)$$

In the designed filter, $R = 4 \text{ M}\Omega$ (high-resistive polysilicon utilised) and $C = 10 \text{ pF}$, resulting in $f_c \simeq 3.98 \text{ kHz}$.

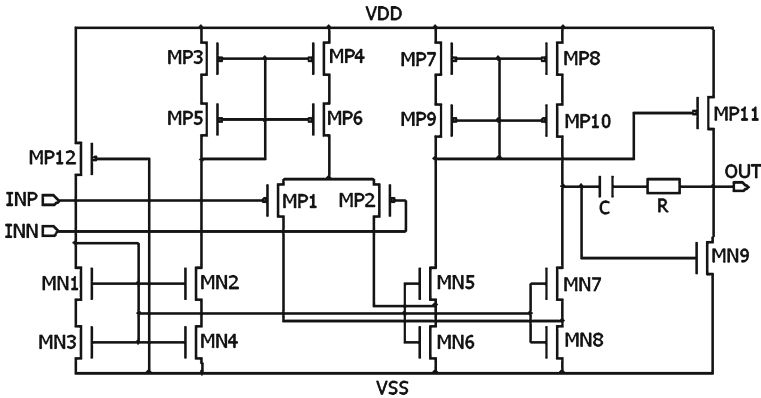


Fig. 9 Designed folded cascode amplifier circuit

The operational amplifier, deployed in all circuits presented in this section, is based on the classic folded cascode architecture (introduced by Choi et al. in [5]). This one—in comparison with the other amplifier architectures—provides higher gain, wider input voltage range and minimisation of the Miller effect for input transistors gate–drain capacity. The schematic of designed cascode circuit is shown in Fig. 9.

3.5 Phase Shift Issue

As it was mentioned in Sect. 2, the delay introduced by the AC amplifier (see Fig. 2) results in a degradation of the overall chopper amplifier gain. To prevent this phenomenon, the phase shift between the modulator and demodulator control signals must follow mentioned delay. Therefore, the phase characteristic of the applied gain stages requires a deeper analysis.

The AC amplifier shown in Fig. 2 has been implemented as two different gain stages: Gm-C filter in each channel and bandpass multiple feedback amplifier in the common part of signal path. The delay introduced by the applied bandpass Gm-C filter can be determined from the transfer function given by the Eq. (6) in Sect. 3.3. By assuming $s = j \cdot \omega$ and $L = \frac{C_L}{g_{m3} \cdot g_{m4}}$, this formula can be rewritten as: (19)

$$\frac{V_{out}}{V_{in}}(\omega) = \frac{j\omega \frac{g_{m1}}{C}}{\frac{1}{LC} - \omega^2 + j\omega \frac{g_{m2}}{C}} \tag{19}$$

The phase characteristic of the Gm-C filter is the argument (phase) of the complex number described by the above equation. For $\omega = 0$ it is equal to 0, but if only the pulsation starts to increase, the phase reaches 90°. For $\omega = \omega_0 = \sqrt{\frac{1}{LC}}$, it is equal to 0, and when $\omega \rightarrow \infty$, it tends to the -90° asymptote. However, these calculations change if the non-idealities of used circuit components are taken into account. The equivalent circuit of the on-chip capacitors consists of many parasitic elements, for example, plate-substrate capacitance or series resistances. Moreover, designed Gm-

blocks have to be characterised by not only their transconductances, but also parasitic nonzero output conductances. All of these non-idealities cause additional, parasitic poles and zeroes in the Gm-C filter transfer function (19). Since the parasitic zeros and poles are located at higher frequencies than the band of transfer function, for single transconductor these effects can be modelled with a single equivalent zero [21]. This zero can be located in either the right complex half-plane (RHP) or the left complex half-plane (LHP), modelling, respectively, phase lag or lead. The exhaustive analysis of equivalent zero impact on transconductor transfer characteristic has been described in several books and articles (e.g. [21] or [26]).

For the bandpass multiple feedback amplifier, the ideal transfer function is given by the Eq. (12). Like in the previous case, this formula can be presented as the complex function of the pulsation ω : (20)

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = \frac{-j\omega C \frac{R_2 R_3}{R_1 + R_3}}{1 + j\omega C \frac{2R_1 R_3}{R_1 + R_3} - \omega^2 C^2 \frac{R_1 R_2 R_3}{R_1 + R_3}} \quad (20)$$

The phase function has a similar character to the Gm-C filter one; however, the MFB amplifier is an inverting circuit. For $\omega \rightarrow 0$, the phase tends to -90° and with increasing pulsation it starts to decrease, reaching -180° (which is identical to the 180°) for $\omega = \omega_0 = \frac{1}{C} \sqrt{\frac{R_1 + R_3}{R_1 R_2 R_3}}$. When $\omega \rightarrow \infty$, phase tends to the -270° asymptote (identical to the 90°). However, the non-idealities of circuit components impact the amplifier transfer function. The on-chip resistors and capacitors contain several parasitic elements, like capacitors to substrate or series resistances, which affect transfer and phase characteristics by adding extra poles and zeroes. The applied operational amplifiers also can be characterised by the nonzero output resistance and capacitance. From the phase shift point of view, the phenomenon called slew-induced distortion (SID) [1] can have a significant impact on a circuit operation. If an operational amplifier is overdriven by a large input signal, the output slew is limited by internal currents and capacitances. When the output signal is forced to exceed this limit, a distortion occurs causing a phase shift and an attenuation of the fundamental component of the output signal. However, this distortion is strongly related to the amplitude of the amplifier differential input signal. When the input voltage reaches a certain threshold, distortion increases [24]. In proposed readout circuit, amplitudes of the multiple feedback amplifier input signals are relatively small—they are microvolt signals from FET-based THz detectors modulated and amplified 100 times by the Gm-C filter. This leads to the conclusion that slew rate of the designed operational amplifier is sufficient to prevent described slew-induced distortion.

From the external control signals generation point of view, the optimal configuration occurs when exactly the same signal is fed to both modulator and demodulator circuits. Therefore, the crucial issue is to determine the pulsation (frequency), for which the phase shift—introduced by the cascade connection of the Gm-C filter and multiple feedback amplifier—is equal to zero. The differential inputs of each Gm-C filter must be connected inversely to the modulators outputs—to meet the resonant pulsation -180° phase shift caused by the MFB. It can be assumed that the overall zero phase shift pulsation is located around the nominal resonant pulsation of both bandpass

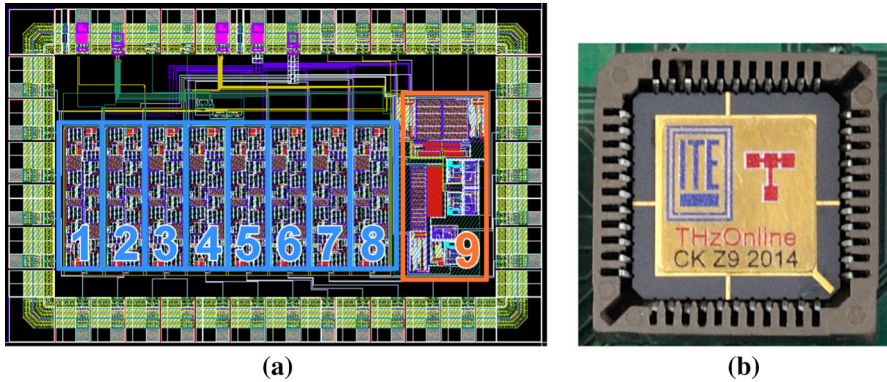


Fig. 10 Designed multichannel IC: **a** layout overview [4×2.5 (mm)] and **b** fabricated chip assembled in LCC44 package and placed in dedicated socket

circuits. The authors performed several post-layout and variation simulations to take into account the impact of the circuit non-idealities and parasitics and to keep this frequency close to the nominal f_{chop} , set to 200 kHz. During the samples measurements (described below in Sect. 4), this parameter has been determined for each tested chip.

3.6 Chip Summary

The presented IC has been fabricated in the standard, cost-effective AMS C35 silicon process (350 nm) with 3.3 V power supply. Figure 10 shows designed layout and chip assembled in LCC44 package. The preamplifiers for each particular channel are marked with numbers from 1 to 8, and number 9 corresponds to the output amplifier—common part of the signal path. For additional isolation from external radiation and interference, all structures were covered by grounded top metal layer.

4 Electrical Measurements

The dedicated test set-up for multichannel readout circuit was developed. Due to the required processing of very small signals, special attention was paid to minimise the reception of external interferences, as well as to limit the noisy digital part of the test set-up to the clocking signal generators only. The test set-up, presented in Fig. 11a, is fully shielded in a metal enclosure, with battery power supply located inside. Typical design practices, like supply line separation, careful decoupling and current flow directing in metal fill layers, were applied to minimise parasitic coupling and interferences propagation. For the crosstalk and dynamic (switching characteristic) measurements, the four of eight input signal pairs are available at the front panel. The special circuit block is added to enable experiments with input and output offset compensation.

All characteristics presented below have been obtained for one of the tested chip samples. At the beginning, the frequency for the AC amplifier zero phase shift has been determined. Then, transfer and input noise characteristics have been measured. Tab. 2, placed at the end of this section, shows the variations of the gain values and

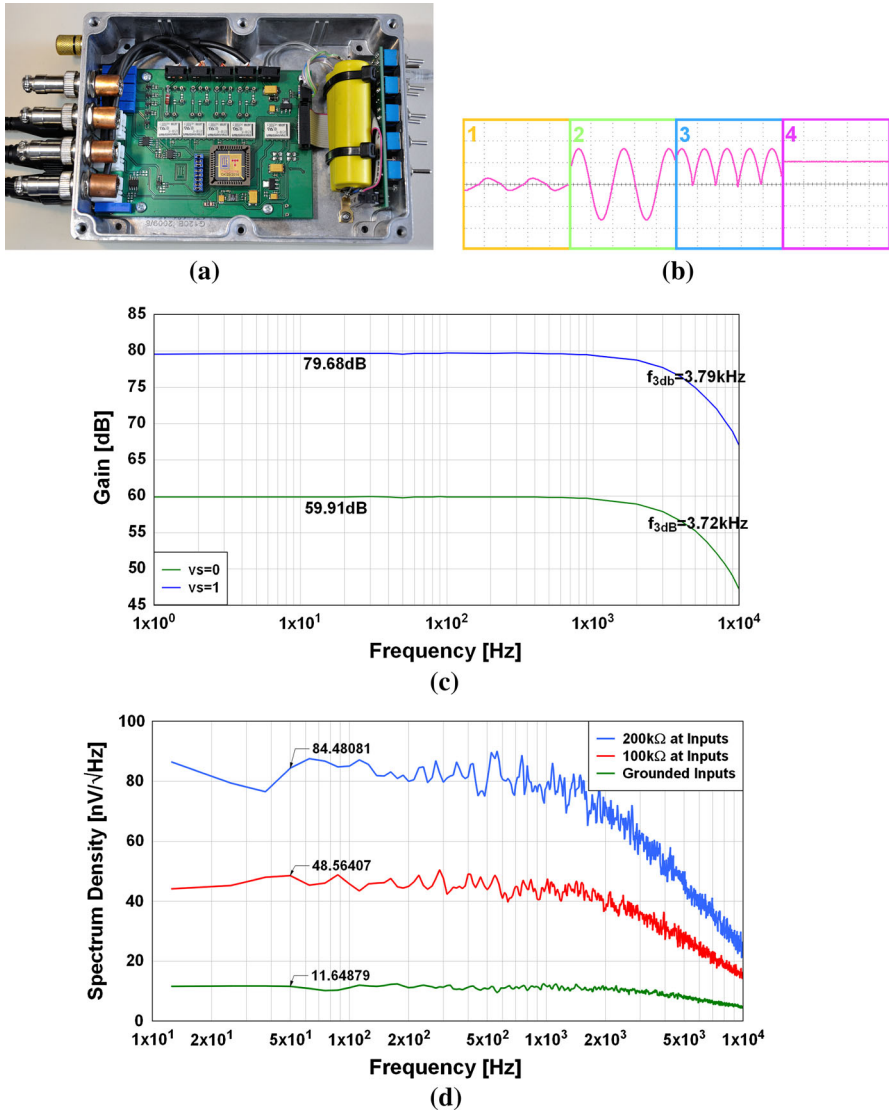


Fig. 11 Electrical measurements of designed IC: **a** dedicated test set-up (top cover removed), **b** internal signals from the IC, **c** transfer curve for channel #0 depending on the versus control signal and **d** input spectral noise density (channel # 0) for shorted input, 100 and 200 k Ω connected to the inputs

zero phase shift frequencies for four measured samples. Small values of the standard variation prove that results obtained for one chip sample are representative for the others.

In Fig. 11b, the internal signals of the designed IC, available via test outputs, are presented. Obtained results are in perfect matching with the theory described in Sect. 2. The numbers above the traces correspond to the internal signals output shown in

Fig. 3 (1—after multiplexer; 2—after 2nd gain stage; 3—after demodulator; 4—after LP filter).

The transfer characteristics for exemplary channel of the readout circuit are shown in Fig. 11c. During measurement process, it has been proven that the transfer curves for all the eight channels are almost identical—each of them is characterised by the bandwidth approximately equal to 3.7 kHz. The gain of the circuit can be changed between 60/80 dB by means of a single control signal affecting the structure of the MFB amplifier resistors ladder.

Figure 11d presents the input noise density curves, taken for three different configurations: with both differential inputs shorted to the ground and with the 100 k Ω /200 k Ω resistor connected between them. Presented results once again prove the main advantage of the chopper stabilisation—significant reduction of the $1/f$ noise component. It is also worth to notice that the noise level equivalent to the thermal noises of applied precise resistors is consistent with theoretical equation $\bar{u}^2 = 4k_B T R \Delta f$.

The crosstalk measurements were also performed but even for the worst case (2 channels located contiguously in the layout), the crosstalk was below the sensitivity of utilised test equipment.

All presented results have been obtained with calibration signals (C1...C8 an CAL in Fig. 3) equal to 0 V. The achieved worst case results (5 μ V) guarantee that the circuit can be used for measurements without the noticeable impact of the input offset.

Table 1 presents the brief comparison between designed circuit and selected comparable solutions that can be used for FET-based THz detectors measurements (or for very low-voltage measurements in general).

AD8574, ICL7652 and LTC1052 are high-precision, commercially available off-the-shelf operational amplifiers. It has to be stressed that for these circuits the maximum gain and 3 dB bandwidth values presented in Table 1 (and marked with *) are related to the open-loop cases. Parameters in the specific applications are determined by the externally added components of the feedback loop. ICL7652 and LTC1052 uses internal chopper stabilisation technique. All of these three circuits are just operational amplifiers and require several external components for proper operation. The IC proposed in this paper is a complete, independent readout system, that needs only external control signals generation (and optionally an input offset compensation circuit—if it is required by a target application).

The SR124 is a complete and expensive lock-in amplifier, from Stanford Research Systems, offering excellent sensitivity and noise parameters. However, the major drawback of this type of measurement equipment is requirement for the THz source modulation and constant synchronisation between the modulated source and the readout circuit.

In [12] the authors present the single-channel readout circuit on-chip integrated with a FET-based detector. This architecture, like the one proposed in this work, is based on the chopper amplifier concept, and additionally equipped with the output $\Sigma\Delta$ converter. It is a promising solution, but the authors presented only simulation results, not confirmed by measurements of fabricated prototypes. The main advantage of this readout is an internal AD converter and very low-power consumption. On the other hand, the achieved input-referred noise

Table 1 Comparison between main parameters of proposed IC and selected comparable solutions

Readout circuit	Input channels	Maximum gain	3 dB bandwidth	Max input offset (μV)	Input noise density
This work	8	80 dB	0–3.7 kHz	5	$11.6 \frac{nV}{\sqrt{Hz}}$ (at 10 Hz)
AD8574 [2]	4	145 dB*	0–85 mHz*	5	$51 \frac{nV}{\sqrt{Hz}}$ (at 1 kHz)
ICL7652 [34]	1	150 dB*	0–60 mHz*	5	$94 \frac{nV}{\sqrt{Hz}}$ (at 10 Hz)
LTC1052 [19]	1	150 dB*	0–38 mHz*	5	$500 \frac{nV}{\sqrt{Hz}}$ (at 1 Hz)
SR124 [31]	1	160 dB	0.2 Hz–200 kHz	–	$2.5 \frac{nV}{\sqrt{Hz}}$ (at 1 kHz)
[12]	1	40 dB	0–1 kHz	–	$87.5 \frac{nV}{\sqrt{Hz}}$ (at 10 Hz)
[6]	1	50.5 dB	0.5 Hz–100 Hz	–	$100 \frac{nV}{\sqrt{Hz}}$ (at 100 Hz)

density is substantially higher than in solution described in this paper though. Moreover, that circuit is a single-channel solution, offering significantly lower gain.

For a better comparison, an integrated chopper amplifier front-end for bio-signals processing has been added to the Table 1 [6]. Many requirements for a biological sensing readout are quite similar to the target parameters for FET-based detectors. However, the major difference between these two applications is in a DC signal processing. The bio-signal front-ends are required to treat any DC signal as unwanted and hence to reject it, while the ones operating with FET-based THz detectors, which output signal is a DC, need to amplify this component. Therefore, it is incorrect to directly compare the noise parameters between these two applications, because the DC rejection mentioned above automatically results in a $1/f$ noise component reduction. But even in this case the circuit parameters presented in this work are fully comparable to the majority of the integrated bio-signal sensing front-ends.

Table 2 presents chosen measurement results for four tested samples. The values of a zero phase shift frequency of the AC amplifier have been determined for each of the input channels of the circuit, and then their average was calculated. Next, the circuit gain was measured for the chopping frequency determined in the precious step.

Table 2 Measurement results for four chip samples: zero phase shift frequency and gain value for $v_s = 0/1$

Sample	Channel	f_0 (kHz)	Gain ($v_s = 0$) (dB)	Gain ($v_s = 1$) (dB)
#1	0	210.3	59.91	79.68
	1	210.6	59.89	79.53
	2	209.9	59.86	79.63
	3	210.7	59.92	79.61
	4	210.1	59.89	80.29
	5	209.8	59.86	80.36
	6	210.3	59.85	80.33
	7	210.4	59.86	80.38
#2	0	208.7	59.78	79.03
	1	209.0	59.89	79.63
	2	208.5	59.95	79.16
	3	209.5	59.90	79.77
	4	208.6	59.90	79.97
	5	208.4	59.84	79.89
	6	208.8	59.83	79.85
	7	208.8	59.84	80.25
#3	0	209.8	59.82	80.15
	1	210.0	59.90	80.09
	2	209.4	59.94	80.44
	3	210.2	59.96	80.22
	4	209.4	59.86	80.87
	5	209.3	59.85	81.42
	6	209.8	59.90	80.96
	7	209.9	59.82	81.44
#4	0	208.5	59.54	79.88
	1	208.7	59.55	80.13
	2	208.2	59.48	80.40
	3	209.3	59.58	80.01
	4	208.3	59.52	80.71
	5	208.2	59.51	81.27
	6	208.6	59.55	80.84
	7	208.5	59.53	81.36
Average		209.35	59.79	80.20
SD		0.78	0.16	0.59

5 THz Measurements

The IC described in this work has been also tested in its target application—with eight FET-based detectors connected to the inputs and illuminated by the THz radiation. To

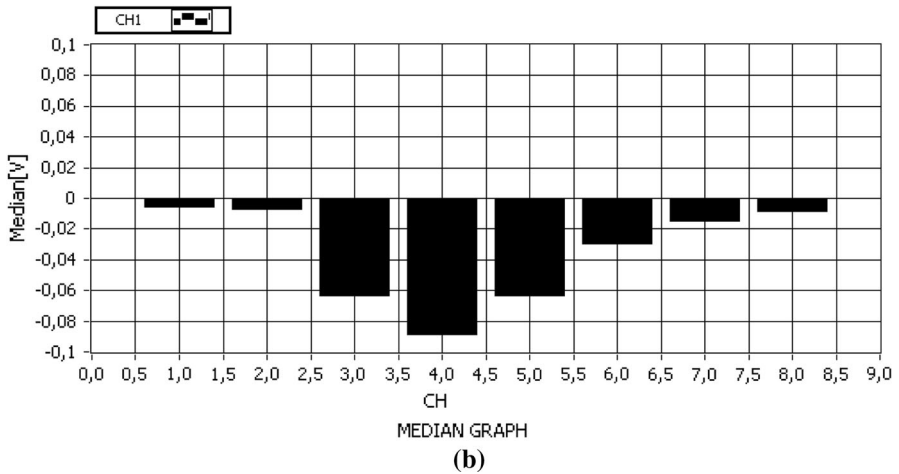
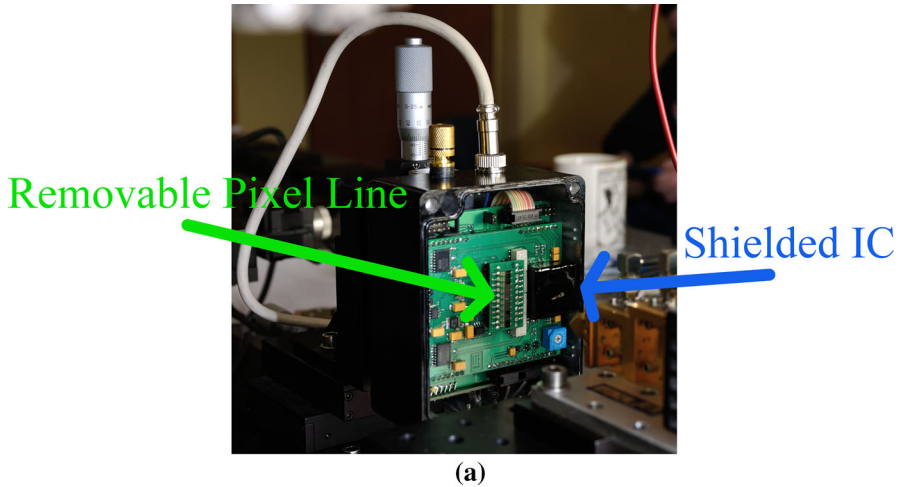


Fig. 12 THz measurements of the designed IC: **a** dedicated test set-up and **b** measurement results for 8-detector line, THz beam centred on the fourth pixel

perform this type of measurement, another dedicated test set-up, presented in Fig. 12a, has been developed.

This test set-up is a complete device, enabling measurements of the 8-element detector lines assembled, for the convenience sake, on the separate, removable PCBs. This allows easy replacement of the detector set, toward different needs of the research to be performed. Several data converters, supervised by the 8-bit MCU, are used to control the analog settings of the IC under test and to digitise the analog output of the chip. The MCU communicates with the PC through the USB interface and the dedicated application for NI LabVIEW™ provides convenient user interface for setting the measurement parameters and visualisation of gathered data.

Figure 12b shows exemplary measurements results obtained using the set-up described above, with a sub-THz beam (340 GHz) centred on the fourth pixel. The

gain of the IC was set to 60 dB. Presented bar chart shows the output signals from the subsequent detectors, denoted by the numbers under the trace. For each pixel, 2000 samples have been gathered, and their median has been calculated and presented in a form of a single bar. The achieved values are negative due to the fact that the output buffer of the designed IC inverts phase of its input signal. In this way, Fig. 12b illustrates the power distribution across THz beam (in a vertical direction).

It must be mentioned that during the THz measurements no beam modulation nor lock-in amplifier has been used. According to the output signals presented in Fig. 12b (obtained with 60 dB gain), amplitude of input signals coming from FET detectors was roughly tens of μV . The presented IC ensures successful signal processing of these very small DC signals, without necessity of using the phase-sensitive detection. This was the main goal of designed circuit, according to the design objectives presented in Sect. 1.

6 Conclusion

In this paper, the authors described the dedicated readout IC for FET-based THz detectors. It has been experimentally proven that proposed chip can successfully replace the lock-in equipment and may be used for processing of very small, DC signals. Due to this fact, presented solution provides a unique approach to FET-based THz detectors readout and opens up the way for the new possibilities in the field of miniaturisation of the THz imaging systems. Nowadays, most experimental studies concerning characterisation of FETs for THz applications are performed using lock-in technique, which requires expensive, stationary measurement equipment. Proposed readout technique, based on the chopper stabilisation concept, eliminates the need of THz wave modulation and can be used for integration of the readout functionality in a single chip, which can be efficiently applied in miniaturised, even portable devices.

Moreover, the proposed IC is a very universal device and it can be used in many other systems, performing a role of the readout circuit for signal sources other than the mentioned FET-based detectors. Described chip has a great potential to play an important role in a processing of a very small, low-frequency signals, where lock-in technique is commonly used nowadays. Very good example of this kind of applications is noise measurements, experiments performed in very low temperature (cryogenic) or many biomedical signals registration. However, in these cases an additional DC rejection mechanism has to be implemented.

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