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Guest Editorial: Low-Power Digital Filter Design Techniques and Their Applications

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Welcome to this Special Issue on Low-Power Digital Filter Design Techniques and Their Applications. Digital filters are essential elements of many signal processing systems and everyday electronics such as radios, cell phones, and biomedical devices. With the ever-increasing popularity of portable devices in communication, medical, and audio/video systems, the computational efficiency and power consumption of digital filters have become increasingly a matter of concern, as digital filters usually involve a large number of arithmetic operations, especially for the finite impulse response (FIR) filters.

While FIR filters do have merits in stability, linear phase property, and low coefficient sensitivity, they consume more power than their infinite impulse response (IIR) equivalents in general. There has been consistent effort to develop low-power techniques for FIR filters in the past half century, such as multirate filtering, subfilter approaches, and multiplierless filtering. In multirate filtering, arithmetic units are shifted to the lower frequency end, resulting in reduced power at low operation frequencies. In subfilter approaches, filters are connected in series and/or parallel to form a network, where the frequency responses of different frequency intervals are taken care of by different filters or filter pairs. The overall number of non-trivial coefficients can be significantly reduced by cleverly arranging the subfilters. A very successful subfilter structure is the frequency-response masking (FRM) structure, which was first proposed in 1986 by Y.C. Lim. In 1979 Lim pioneered multiplierless filter-

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ing as well. Full-fledged multipliers are not required when filter coefficient values are represented as a sum of a limited number of signed power-of-two terms.

The original ideas of multirate filtering, subfilter approaches, and multiplierless filtering have been continuously perfected over the past decades. The above-mentioned techniques originally developed for FIR filter design have been subsequently applied to IIR filter design. New applications emerge as the power consumption of digital filters shrinks. This Special Issue is a collection of state-of-the-art design techniques in digital filter structures, optimizations and architectures, and their applications. As a forum for researchers exchanging their latest findings, this Special Issue serves as a platform to create a momentum for new development and breakthroughs in this exciting area.

This Special Issue containing eight papers addresses low-power filter design issues, from filter structures and multiplier-free coefficient optimization, to filter banks and filter architectures. In the first group of three papers discussing filter structures, the first one presents a new serial masking scheme for the synthesis of FRM-based filters. The second paper presents a novel untraditional piecewise-polynomial impulse response filter structure. Presented in the third paper is a digital filter design system that provides a way to systematically explore different IIR filter structures. The second group of two papers presents the latest developments in multiplierless filter design. In one of the papers, adders are shared among coefficients when filter coefficients are represented as a sum of a limited number of subexpression terms, while the other paper introduces a bit-level optimization to reduce the number of pipelined partial products in the generation of coefficient multipliers. In the third group of two papers, one proposes two classes of low computational complexity cosine-modulated filter banks, while the other applies low-power filter banks for the design of quality analog scramblers. Last but not least, a low-power resampling architecture is proposed for particle filters. The following is a brief sketch of each of the eight articles.

The first paper, "Frequency-Response Masking Filters Based on Serial Masking Schemes," by Y. Wei and Y. Lian, proposes a computationally efficient filter structure based on the FRM technique for the synthesis of arbitrary bandwidth sharp FIR filters. A serial masking scheme, instead of the traditional parallel one, is introduced to perform the masking tasks in two stages, resulting in a reduction in the complexity of masking filters. Compared to the original FRM, the proposed structures achieve additional savings in terms of numbers of arithmetic operations.

The second paper, "Synthesis of Wideband Linear-Phase FIR Filters with a Piecewise-Polynomial Sinusoidal Impulse Response," by R. Lehto, T. Saramäki, and O. Vainio, presents a piecewise-polynomial sinusoidal impulse response to synthesize wideband linear-phase FIR filters. The desired impulse response is created by using a parallel connection of several filter branches and by adding an arbitrary number of center coefficients. This method is especially effective to design Hilbert transformers with one or two transition bands with equal widths. The arithmetic complexity is proportional to the number of branches, the common polynomial order for each branch, and the number of separate center coefficients. Examples show the advantages of this method over the FRM technique in the terms of number of coefficients.

The third paper, "Digital Filter Design Using Computer Algebra Systems," by M.D. Lutovac, J.D. Ćertić and L.D. Milić, introduces a computer algebra system for

algorithm development and digital filter design. The main result of the paper is the development of an algorithm for IIR filter design that, theoretically, is impossible to implement using the traditional approach. In a systematical way, a known multiplierless digital filter is used as a startup to design a new digital filter whose passband edge frequency can be simply adjusted by using a single parameter. As a result, a multiplierless IIR filter could be realized by using a small number of adders.

The fourth paper, "Optimization of Linear Phase FIR Filters in Dynamically Expanding Subexpression Space," by Y.J. Yu and Y.C. Lim, considers common subexpression sharing when the filter coefficients are optimized. Common subexpression sharing is the most advanced technique for multiplierless filtering. Based on the concept of subexpression space, in this paper, a tree search algorithm is proposed to update and expand the subexpression spaces dynamically and, thus, to achieve the maximum sharing during the optimization. Numerical examples show the savings in the number of adders achieved by the proposed technique.

The fifth paper, "Integer Linear Programming-Based Bit-Level Optimization for High-Speed FIR Decimation Filter Architectures," by A. Blad and O. Gustafsson, considers the implementation of decimation filters in a polyphase structure for sigma-delta modulation. The filters are implemented with an efficient partial product generation and mergence. A bit-level optimization algorithm is proposed to efficiently reduce the pipelined partial product. A comparison between the main architectural choices for FIR filters: the direct-form and transposed direct-form structures, is presented. The optimization results are complemented with energy dissipation and cell area estimations for a 90 nm CMOS process.

The sixth paper, "Two Classes of Cosine-Modulated IIR/IIR and IIR/FIR NPR Filter Banks," by L. Rosenbaum, P. Löwenborg, and H. Johansson, introduces two classes of cosine-modulated causal and stable filter banks (FBs) with near perfect reconstruction and low implementation complexity. Both classes have the same IIR analysis FB but different synthesis FBs utilizing IIR and FIR filters, respectively. The two classes are preferable for different types of specifications. The paper provides systematic design procedures so that perfect reconstruction can be approximated as closely as desired. It is demonstrated through several examples that the proposed FB classes, depending on the specification, can have a lower implementation complexity compared to existing FIR and IIR cosine-modulated FBs.

The seventh paper, "Quality Analog Scramblers Using Frequency Response Masking Filter Banks," by Y.C. Lim, J.W. Lee, and S.W. Foo, proposes a very low complexity frequency-domain analog speech scrambler having high-quality speech reconstruction. The scrambler uses FRM filter banks which have low computational complexity and narrow transition widths. The proposed system does not require bandwidth expansion and is robust for transmission channels with distortion characteristics. Preliminary investigations showed that speech scrambled using this method is nearly unintelligible to the casual eavesdropper.

The last paper, "A Low-Power Memory-Efficient Resampling Architecture for Particle Filters," by S.H. Hong, Z.G. Shi, J.M. Chen, and K.S. Chen, proposes a compact threshold-based resampling algorithm and architecture for efficient hardware implementation of particle filters. By using a threshold-based scheme, the proposed resampling algorithm reduces the complexity of hardware implementation and

power consumption, while the performance is comparable to that of the traditional systematic resampling (SR) algorithm. An experimental comparison of the proposed hardware architecture with those based on the SR and residual systematic resampling algorithms was conducted on a Xilinx Virtex-II Pro FPGA platform in the bearings-only tracking context, and the results establish the superiority of the proposed architecture in terms of high memory efficiency, low power consumption, and low latency.

We thank all the authors for their contributions and we express our deepest gratitude to the reviewers for their time and effort in maintaining the quality of this Special Issue. We also express our sincere appreciation to the Editor-in-Chief, Dr. M.N.S. Swamy, for his support in developing this Special Issue.

Guest Editors
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Dr. Lian has been involved in various IEEE activities. He has served as the Vice President for Asia and Pacific Region of the IEEE Circuits and Systems (CAS) Society (2007–2008), IEEE CAS Society Representative to the BioTechnology Council (2007–present) and the IEEE Biometrics Council (2008–present), Chair of the Biomedical Circuits and Systems (BioCAS) Technical Committee (2007–2009) and Secretary of the DSP Technical Committee (2008–present) of IEEE CAS Society, Steering Committee Member of the *IEEE Transactions on Biomedical Circuits and Systems* (*TBioCAS*) (2007–present), Panel Judge of Student Paper Contest in the IEEE International Symposium on Circuits and Systems (2007), member of Prize Paper Award Subcommittee for the IEEE CAS Society (2007), Distinguished Lecturer of the IEEE CAS Society (2004–2005), and Chair of the IEEE International Steering Committee of Asia Pacific Conference on Circuits and Systems (2007–2008). He has served as Associate Editor for the *IEEE Transactions on Circuits and Systems Part II* (*TCAS-II*) (2002–2003), Associate Editor for the *IEEE TCAS-I* (2004–2005), Associate Editor for the *IEEE TCAS-II* (2006–2007), Associate Editor for the *IEEE TCAS-I* (2008–present), Associate Editor for the *IEEE TBioCAS* (2007–present), Associate Editor for the journal *Circuits, Systems, and Signal Processing* (*CSSP*) (2000–2009), Guest Editor of the *IEEE TBioCAS* for the Special Issue on selected papers for ISCAS'2007 (Dec. 2008), Guest Editor of the journal *CSSP* for the Special Issues in 2003 and 2005, and Guest Editor of the *IEEE TCAS-I* for the Special Issue on Biomedical Circuits and Systems: A New Wave of Technology (Dec. 2005). He is the co-founder of the IEEE International Conference on Biomedical Circuits and Systems (BioCAS). He has been the General Co-Chair of the BioCAS 2004, Technical Program Co-Chair of the BioCAS 2006, Tutorial Chair of the BioCAS 2007,

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