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Recent progress in gold nanoparticle-based non-volatile memory devices

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Abstract

Recently, much progress has been made toward the fabrication of non-volatile memory devices based on metallic nanoparticles. Among the many kinds of nanoparticles, gold nanoparticles are some of the most widely used materials for charge trapping elements in non-volatile memory devices because they are chemically stable, easily synthesized, and have a high work function. Various synthesis methods have been applied to fabricate gold nanoparticle-based non-volatile memory devices and recent progress indicates that gold is a very promising material for non-volatile memory applications. In this article, the recent advances in fabrication and characterization of gold nanoparticle-based non-volatile memory devices, with an emphasis on flash memory-type memory devices, are reviewed. Detailed device fabrication, characterization, and future directions are reported based on the recent research activities and literature.

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Keywords: *gold, nanoparticles, memory devices, charge trapping*

1 Introduction

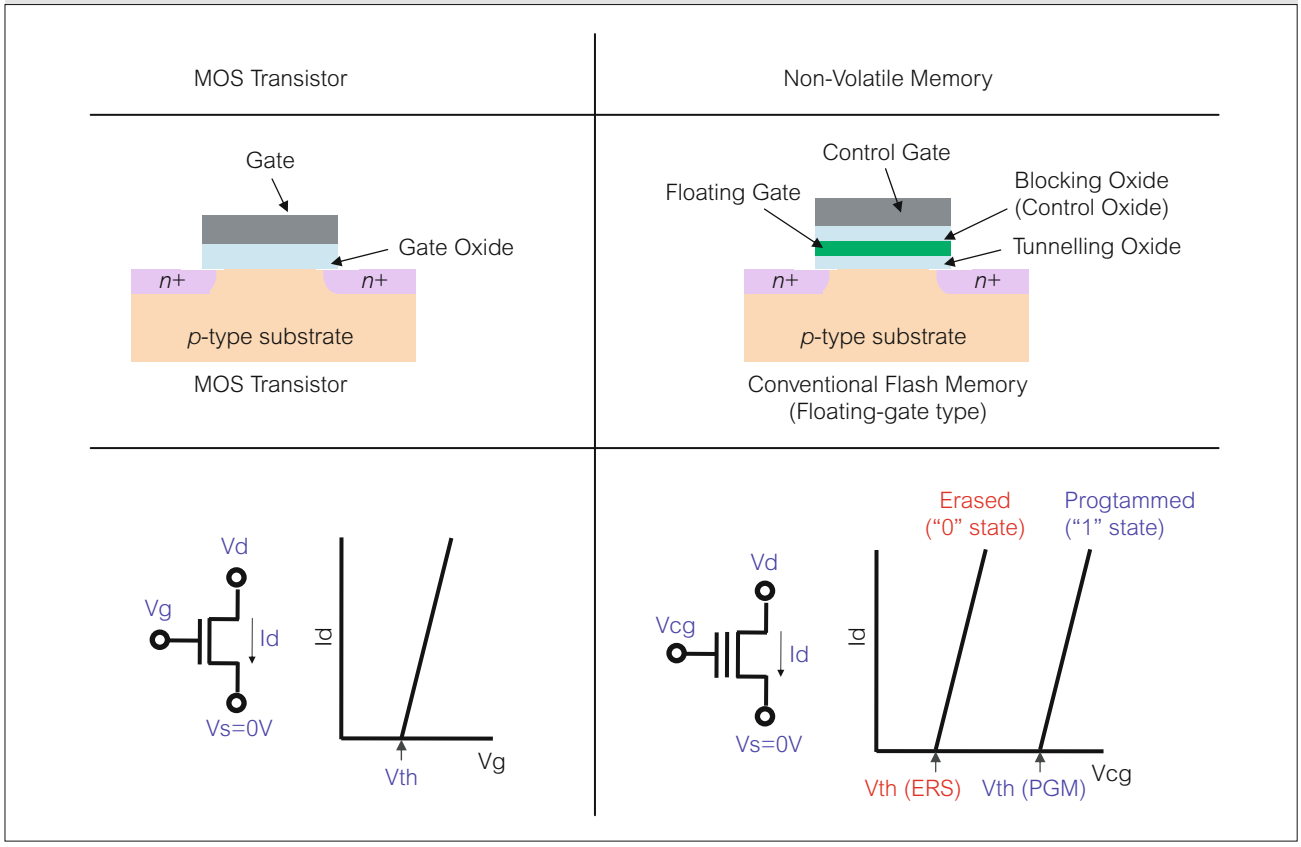
Gold is used for various areas including jewellery, science, and technology [1]. In the areas of science and technology, gold has been used in biomedical applications, catalysis, electrochemical applications, nanotechnology, electronics, etc [2-14]. Significantly, gold has a great potential to be used in semiconductor devices, but its usage is still limited to bonding applications [15,16]. There are many types of semiconductor devices, including logic devices, memory devices, displays, etc. and the market for semiconductor devices is massive and demand is increasing. Among the many types of semiconductor devices, there is a great demand for memory devices with high-density, high-speed, and low power consumption. In addition, non-volatility is important since high-performance and high-density non-volatile memory devices should be integrated with consumer electronic devices (for example, mobile phones, digital cameras, potable media players, laptop computers, etc.). Therefore, tremendous effort has been made toward the development of high-density, low-cost, and non-volatile solid-state storage devices [17-28]. Among the many types of non-volatile memory technology, flash memory devices based on the floating gate have been widely used due to their massive memory capacity, which has been required for many applications [17,19-21,23]. However, floating-gate based flash memory has been reported to have limits in continuous device scaling due to increasing cell-to-cell interference, decreasing coupling ratio, non-scalable tunnelling oxide thickness, decreasing tolerance for charge loss, etc. Therefore, active research has been performed on flash memory devices with discrete charge trapping layers, such as silicon-oxide-nitride-oxide-silicon (SONOS) devices [29-33,25] or nanocrystal (NC)-based memory devices (nano-floating gate memory devices) [34-38]. Because of their better endurance, smaller

chip size, and lower power consumption when compared with floating-gate devices, this technology is of great interest to the electronics industry. Recently, Samsung Electronics reported that they successfully fabricated a 64-gigabit density SONOS-type flash memory device using Si_3N_4 as a charge trap layer. However, it is very difficult to control the trap density and distribution in SONOS devices, although these parameters are quite important in determining the memory characteristics, especially with regards to the programmed/erased bit distribution and data retention. Thus, NC memory devices using semiconducting or metallic NCs as a charge trapping layer have an advantage when it comes to controlling the trap density and distribution, because the density and location of the NCs can be controlled by adjusting the process parameters. Considerable work has focused on the controlled synthesis of semiconducting or metallic nanoparticles for use in non-volatile memory devices. Recently, there have been many reports regarding the fabrication of NC-based memory devices utilizing gold nanoparticles. In this article, recent efforts and research activities regarding the fabrication and characterization of gold-nanoparticle-based non-volatile memory devices are reported. Emphasis is placed on the transistor-based non-volatile memory devices since the device structure is similar to the conventional flash memory devices, thus there is a great opportunity for this technology to be adopted in future flash memory devices as well as novel memory devices (for example, flexible/printed/organic memory devices).

2 Operations of non-volatile memory devices

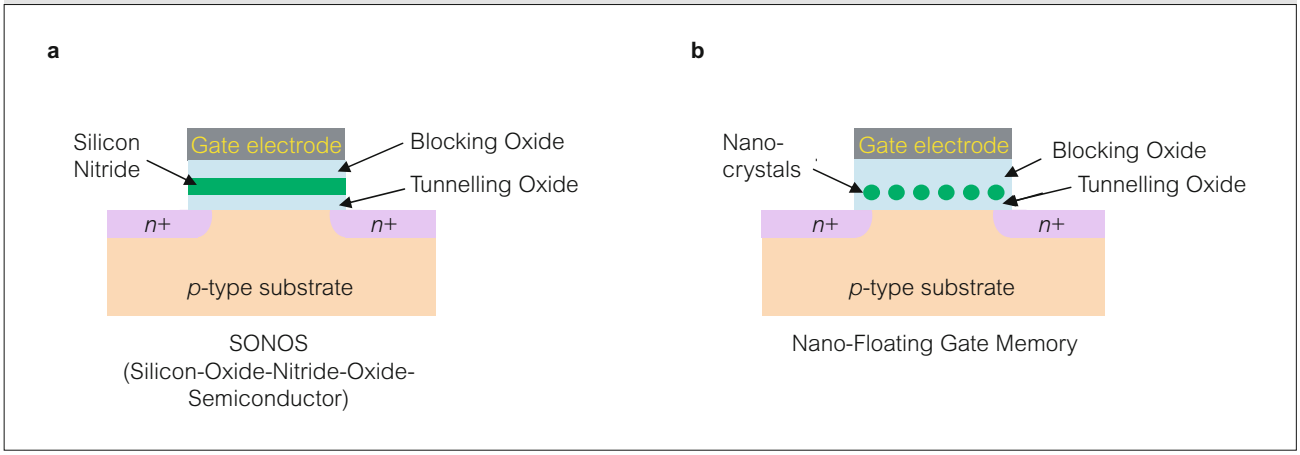
The basic operation of non-volatile flash memory devices is shown in Fig. 1 with comparison to the MOS transistor devices [20]. In the case of ideal MOS transistor devices, the threshold voltage (V_{th}) is fixed at a constant drain voltage (V_d). On the other hand, non-volatile memory devices have charge storage (or trapping) layers, so the charge carriers can be stored (or trapped) in the charge storage layer. A conventional flash memory cell has a floating gate, so the electrons can be stored in the floating gate by the programming operations and moved

Figure 1



Device operation schemes of metal-oxide-semiconductor (MOS) transistors and conventional non-volatile flash memory devices

Figure 2



Schematic device structures of charge trapping flash memory devices. a) Nitride-based memory devices and b) nano-floating gate memory devices

back to the substrate by the erasing operations. According to the programming/erasing operations, V_{th} can be changed since channel conductance is influenced by whether the charge carriers are stored in the floating gate or not. Thus, one can verify the programmed and erased states of the flash memory devices by measuring the drain current (I_d). The erased and programmed states are "0" and "1" states, respectively. Therefore, each flash memory cell can store information as either "0" or "1", which is also 1 bit. Advanced flash memory technology can store more than 1 bit in each flash memory cell, making it possible to increase the memory density further without reducing the cell size. The stored charges are located in the potential well of blocking (or sometimes called control oxide) and tunnelling oxide layers, so the information can be maintained even after the power outage, resulting in non-volatile memory operations [19-21]. This is the major technical advancement that has been made since the invention of flash memory devices using the floating gate. However, as device scaling continues, we face numerous scaling challenges [25]. First, the tunnelling oxide thickness should be reduced, but it is very difficult to scale the tunnelling oxide thickness due to charge retention and stress-induced leakage current. Also, there are serious problems with respect to the distance between cells as they become closer, such as the decrease of the coupling ratio due to the increased parasitic capacitance and increase in cell-to-cell interference. Increased cell-to-cell interference can result in cell V_{th} shift and memory window margin decreases. Furthermore, as the dimensions of floating gates become smaller, the total number of stored electrons in floating gates is reduced, resulting in very tight margins for electron tolerance. Therefore, there is an attempt to solve these problems by changing the charge storage layer from floating gates to insulating silicon nitride (schematic diagram is shown in Fig. 2a). In this case, the problem originating from the use of conducting floating gates can be effectively solved, but the trap levels and trap sites in silicon nitride are not controllable since the charges can be trapped in between conduction and valence bands of silicon nitride. On the other hand, the flash memory devices based on metallic or semiconducting nanocrystals (or nanoparticles) have advantages over floating-gate type flash or silicon nitride-based flash memory devices since the nanocrystal flash memory devices use both devices' advantages (schematic structure is shown in Fig. 2b). First, the nanocrystals (nanoparticles) are deposited on the tunnelling oxide layer discretely, so there is no problem related to the use of a (continuous) conducting floating-gate layer. Second, the trap levels and trap sites can be effectively controlled by manipulating the work function and dimensions (size and density) of the nanocrystals. Thus, many efforts have been made toward the development of nanocrystal-based non-volatile flash memory devices.

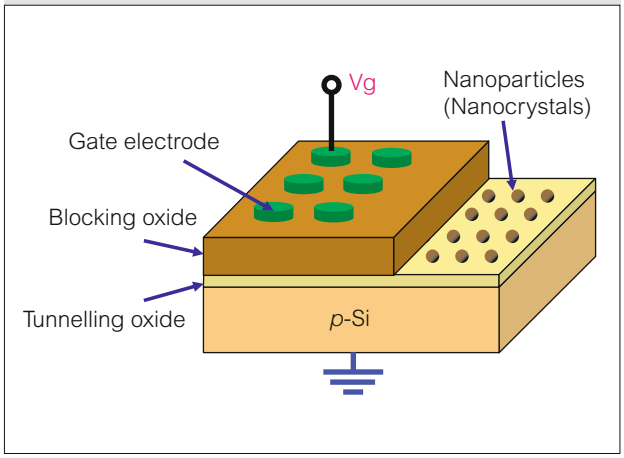
3 Metal-oxide-semiconductor (MOS) structure memory devices

3.1 MOS capacitor-type memory devices

Since MOS capacitor-type flash memory devices can be simply fabricated without source/drain junctions the prototypes of nanocrystal-based memory devices have been fabricated with a MOS-

capacitor structure. The typical structure of MOS-capacitor memory devices is shown in Fig. 3 [39, 40]. Most of the memory devices are fabricated on the p-type Si substrates with a thin tunnelling oxide layer. Metallic nanoparticles are formed on the tunnelling oxide layer. Then, blocking oxide is deposited and, finally, the gate electrode is formed and patterned to make MOS-capacitor structure memory devices. In this case, capacitance-voltage response is used to determine the programmed/erased states. Here, one of the most important device elements is the nanoparticles used as the charge trapping elements. There are various ways to synthesize the metallic nanoparticle-charge trapping elements. Also, many kinds of metallic nanoparticles have been utilized for the applications to the nanoparticle-based memory devices. Among the various species of metallic nanoparticles gold has been reported to be chemically stable, easily synthesized, and have a high work function [41]. Those properties are very important in fabricating nanoparticle-based memory devices as well as ensuring good memory characteristics. Significantly, gold nanoparticles are reported to be synthesized by the Ostwald ripening and chemical solution methods in memory device applications [41]. The synthesized gold nanoparticles should be attached to the tunnelling oxide-covered silicon substrates. The charge trapping layer formation is mostly done by the self-assembly processes. One can synthesize the gold nanoparticle layer by depositing very thin gold layers on the tunnelling oxide-covered silicon substrates. After depositing a thin gold layer, a post-annealing process may be applied to synthesize agglomerated gold nanoparticles by Ostwald ripening. Normally a high temperature annealing process is applied to make gold nanoparticles. In this case, a thin gold layer can be converted to the gold nanoparticles due to the minimization of the surface energy [37]. By adopting this method, gold nanoparticle-based non-volatile memory devices can be fabricated. This is a very simple way to fabricate gold nanoparticle-based memory devices, and the device performance is reported to be good in terms of program/erase characteristics. However, metallic contamination in the gate oxide layer and/or diffusion of metallic components to the interfaces of the memory devices can occur during synthesis of metallic nanoparticles [42]. In addition, the size distribution of metallic nanoparticles is normally very high, the size control is difficult, and generally there are some undetectable nanoparticles, so the calculation of trap density is very difficult. However, the process is compatible with conventional

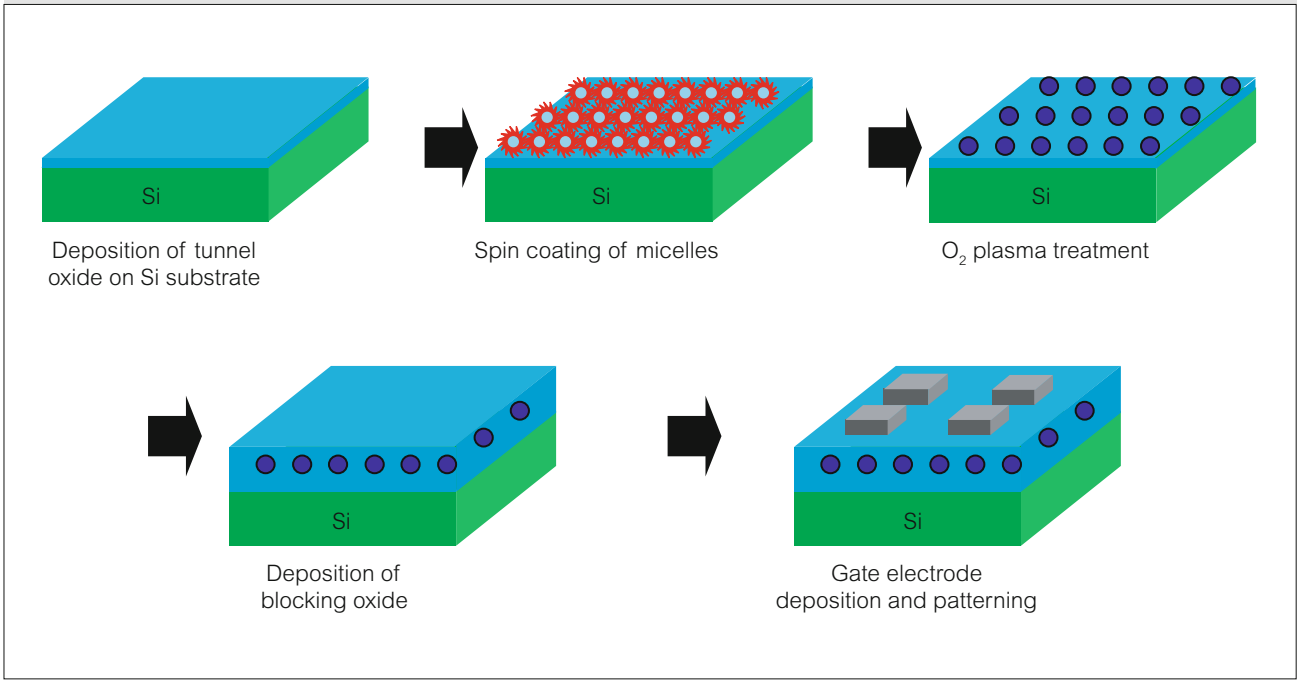
Figure 3



Schematic device structure of MOS capacitor nano-floating gate memory devices

semiconductor device fabrication and one can achieve very high-density nanoparticle layers, thus many studies have been performed using this method. For example, Lee et al. reported on the non-volatile memory effects using self-assembled gold nanoparticles [42]. Thin tunnelling oxide layer (SiO_2 of ~3 nm) was employed and a 1.2 nm-thick gold layer was deposited by e-beam evaporation. After the thermal annealing at 575°C the gold nanocrystal layer was formed. Since very thin tunnelling oxide was used in memory devices, a large memory window could be obtained by the application of low program-erase operating voltages. High dielectric constant (high-k) materials are also reported to be used as gate dielectric layers [43]. The programmable memory characteristics of gold nanoparticle-based memory devices with HfAlO tunnelling/blocking oxide layers are reported. In this report, gold nanoparticles synthesized by the pulsed laser deposition were used and gold nanoparticles were formed in-situ by the substrate annealing during growth (at 300°C and 550°C). Band engineered tunnelling oxide layer (composed of $Al_2O_3/HfO_2/SiO_2$) have been used in gold nanoparticle-based memory devices [44]. Dielectric materials with different bandgaps were deposited in stacks as the tunnelling oxide layer, resulting in increased charge injection efficiencies as well as improved data retention properties. In addition, Kim et al. reported on the use of polymeric insulator layers for both tunnelling and blocking dielectric layers for gold nanoparticle-based non-volatile memory devices [45]. Thin gold film (thickness of 3.4 nm) was deposited on the polyimide (PI)-coated silicon substrates. After the formation of the blocking dielectric layer (PI), the

Figure 4

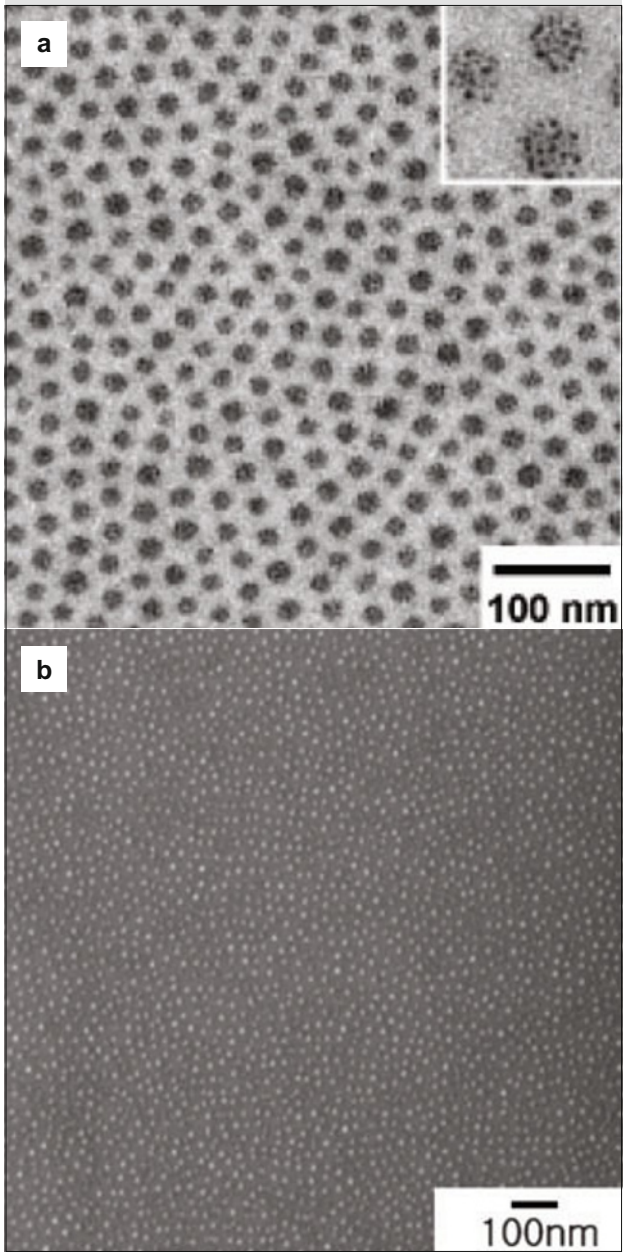


Schematic fabrication processes for typical capacitor-structure nano-floating gate memory devices using diblock copolymer micelle templates. Figures adopted from ref. [39]. Copyright 2007, American Institute of Physics

annealing process was carried out at 400°C to agglomerate gold nanoparticles with a size of around 10 nm. The obtained memory window was 3.4 V at an applied bias of 15 V. On the other hand, there has been active research in the field of nanoparticle-based memory devices using colloidal gold nanoparticles [41]. In this case, the synthesis of gold nanoparticles can be performed in solution, so there is no need to do post-deposition annealing to form metallic nanoparticles [46]. In addition, one can control the size of gold nanoparticles very easily. Another important advantage of using solution-processed gold nanoparticles as the charge trapping layers is the process can be done at very low temperatures, sometimes at room temperature. The solution-processed metallic nanoparticles should be attached to or adsorbed on the tunnelling oxide-covered silicon substrates. Typically, the adsorption can be achieved by the electrostatic interaction between the gold nanoparticles and the adhesion layers. The immobilization of the gold nanoparticle layer is reported to be achieved via the surface modification of the substrates (amine-terminated substrate modification) [47]. The citrate stabilized gold nanoparticles were assembled on the self-assembled monolayer of 3-aminopropyl-triethoxysilane (APTES) and a memory window of around 2 V was obtained at a gate bias of ±10 V.

Diblock copolymers have been used to synthesize controlled gold nanoparticles. Lee et al. reported on controlled synthesis of various metallic nanoparticles using polystyrene-*block*-poly(4-vinyl pyridine) (PS-P4VP) diblock copolymer micelles [39,40]. After assembling micelles embedding gold nanoparticles on the tunnelling oxide-covered silicon substrates, oxygen plasma treatment was carried out to remove the polymer templates. The schematic process steps are shown in Fig. 4 [39]. Then, highly ordered arrays of gold nanoparticles could be achieved. Figure 5a shows the transmission electron microscopy image of the self-assembled micelles deposited by spin coating and 5b shows the scanning electron microscopy image of the gold nanoparticle arrays after removing the micelle templates [40]. The advantage of this technology is easy control of nanoparticle size. By changing the molecular weight of the each block copolymer the resulting nanoparticle size can be controlled. In addition, one can easily synthesize different species of metallic nanoparticle by changing the precursor materials. By using this method the programmable memory properties and reliability of the memory devices were characterized, and, furthermore, by mixing gold nanoparticles with other metallic nanoparticles, tuneable memory characteristics were demonstrated. Leong et al. also reported on the use of PS-P4VP

Figure 5



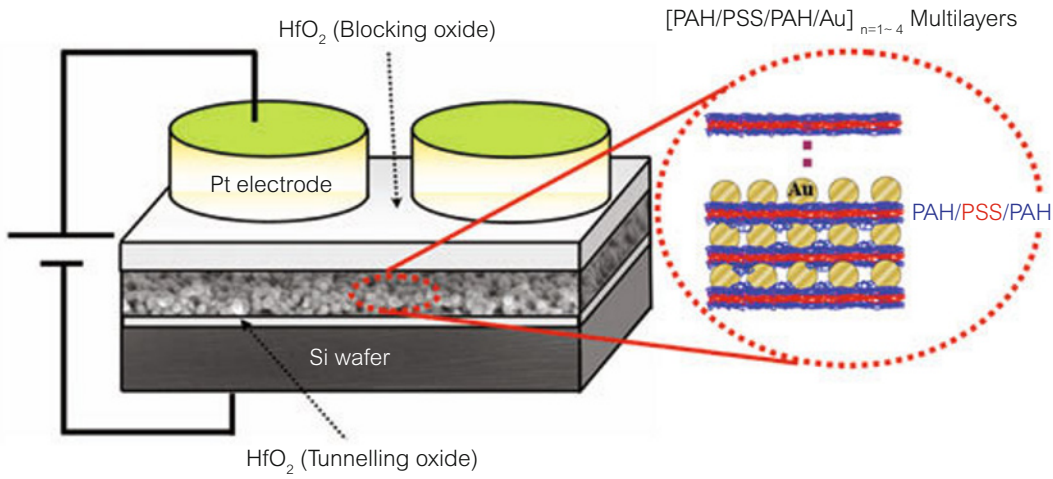
a) Transmission electron microscopy image of spin-coated diblock copolymer micelles with embedded gold nanoparticles. b) Scanning electron microscopy image of the array of gold nanoparticles after removing the micelle templates via oxygen plasma treatment. Figures adopted from ref. [40]. Copyright 2009, Wiley InterScience

diblock copolymer micelles to synthesize gold nanoparticles in MOS-capacitor memory devices, but P4VP core and PS corona block copolymers were not removed since PS and P4VP could be used as the potential well of gold nanoparticles in memory device structures [48]. In addition, there was a report regarding the use of the layer-by-layer (LbL) self-assembly method to synthesize MOS-capacitor structured memory devices. LbL self-assembly is a well-known process, which enables the synthesis of ultra-thin film multilayer by the sequential deposition of each layer with different surface charges. Lee et al. utilized polyelectrolytes with positive and negative charges (poly(allylamine hydrochloride) (PAH) and poly(styrenesulfonate) (PSS)) and negatively charged gold nanoparticles. They sequentially deposited the PAH/PSS/PAH multilayer and gold nanoparticles. By using this method, a charge trapping layer composed of gold nanoparticles could be synthesized by the simple solution dipping processes. Furthermore, they demonstrated facile synthesis of multiple charge trapping layers via solution processes shown in Fig. 6, resulting in a memory window increase [49].

3.2 MOS field-effect transistor-type memory devices

For the real device applications we need transistor-type memory devices since the programmed/erased states can be verified by the drain current. Recently, many efforts have been made on the fabrication of gold-nanoparticle-based transistor-type memory devices. There are two different types of transistor-based memory devices; one is the bulk silicon-based memory device and the other is thin-film transistor-based memory device. The application area will be different according to the types of transistor devices, so memory devices based on bulk silicon can be applied to the conventional silicon-based flash memory device applications, and thin-film transistor-based memory devices can be applied to novel application areas (for example, memory embedded displays, flexible electronic devices, etc.). In the case of transistor-based memory devices, the programmed and erased states can be determined by the measurement of transfer curves (drain current versus gate voltage). By measuring the drain currents at a reading bias, one can determine whether the memory device is in a programmed or an erased state. Most of the fabrication processes described in the MOS capacitor-structure memory devices can be utilized in the synthesis of charge trapping layers composed of gold nanoparticles. Kolliopoulou et al. reported on the use of silicon-on-insulator (SOI) wafers as the substrates and surface modified colloidal gold nanoparticles adsorbed on the APTES-coated tunnelling oxide layers [50]. After the fabrication of source-drain junctions and gate-electrode definition, MOSFET-structure memory devices were fabricated. The average size of gold

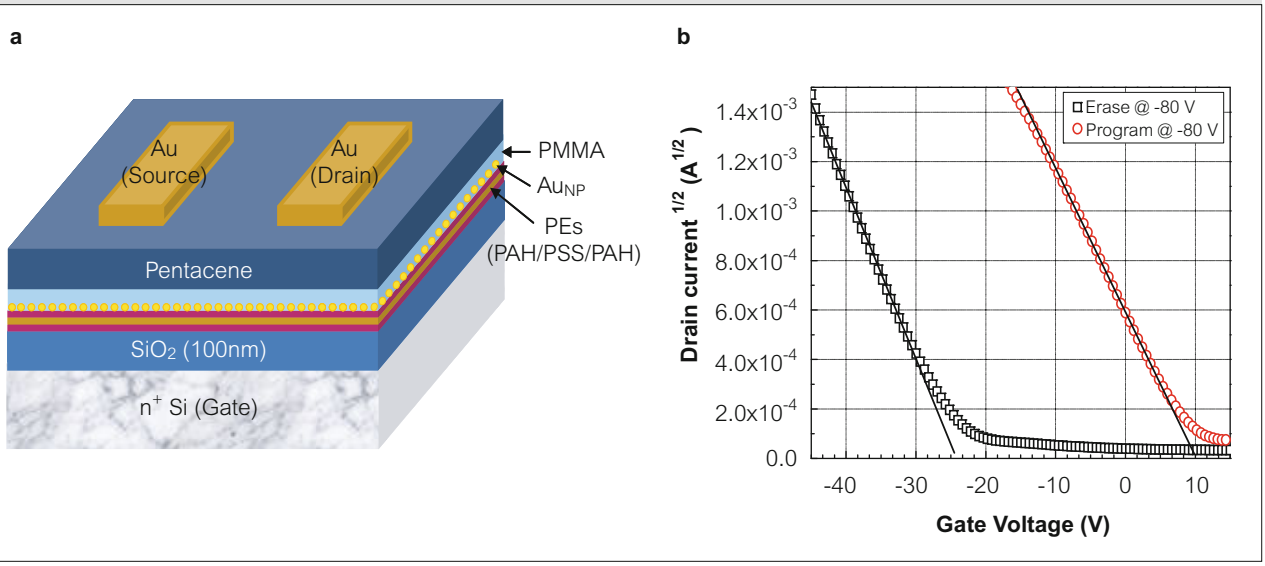
Figure 6



Schematic device structure of capacitor-structure nano-floating gate memory devices with layer-by-layer self-assembled multiple charge trapping layers. Figure adopted from ref. [49]. Copyright 2007, Nature Publishing Group

nanoparticles was around 5 nm and the density was around 5×10^{12} cm^{-2}. They obtained a reasonable memory window of ~6 V by the application of program/erase bias pulses of ±6 V for 1 s as well as good data retention properties. They also reported the use of SiGe active layers to fabricate gold nanoparticle-based nano-floating gate memory devices [51]. Recently, many studies have reported on the use of organic semiconductors as the active layer for MOS transistor-based nano-floating gate memory devices. Liu et al. reported on the use of LbL self-assembled charge trapping layers for nano-floating gate memory devices [52]. They developed bottom-gate and bottom-contact structured nano-floating gate memory devices using spin-coated poly(3-hexylthiophene) (P3HT) as the active layer and ink-jet printed PEDOT/PSS as the source/drain electrodes. Though hysteresis was observed in

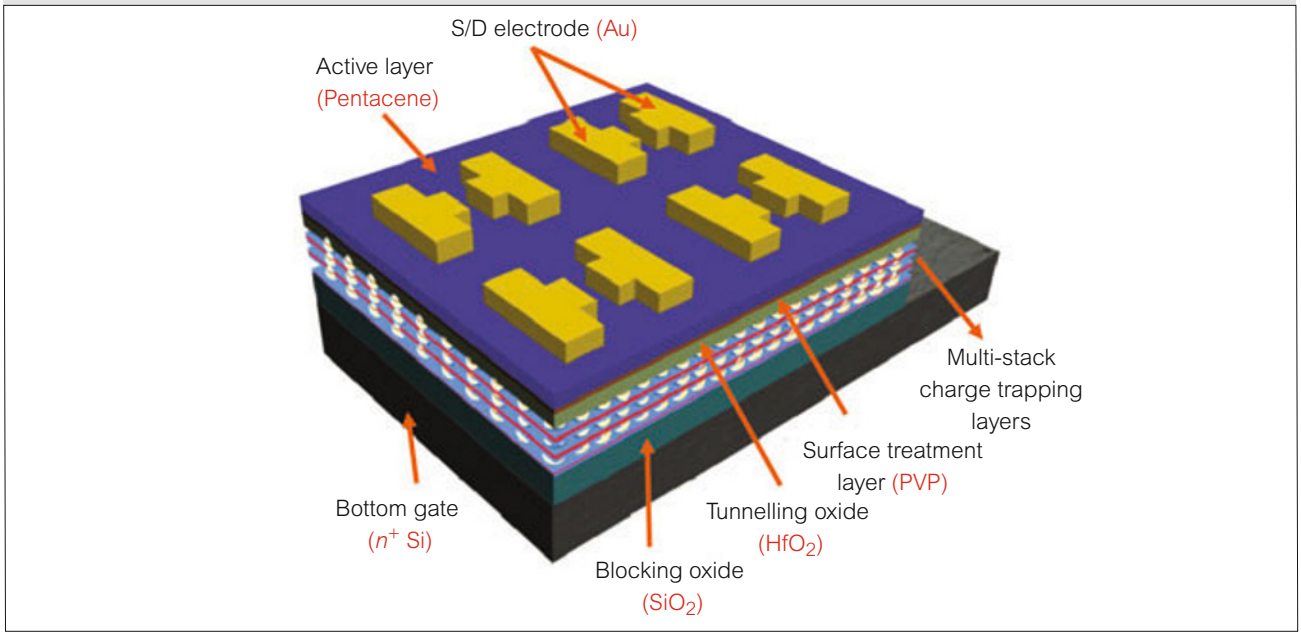
Figure 7



a) Schematic device structure of typical bottom-gate and top-contact structured organic transistor-based nano-floating gate memory devices. b) Program/erase characteristics of the fabricated memory devices. Figure and data adopted from ref. [56]. Copyright 2010, American Institute of Physics

transistor devices without gold nanoparticles, overall the gold nanoparticles were found to be acting as the charge-trapping layer. Pentacene is one of the mostly widely used organic semiconductor materials for use in organic TFTs. Novembre et al. reported on bottom gate (p+Si)/bottom contact (Ti/Au) structured organic transistor-based nano-floating gate memory devices [53]. The colloidal gold nanoparticles were adsorbed onto the amino-terminated self-assembled monolayer surface treated blocking oxide (SiO_2) layer and pentacene was used as the channel layer. Mabrook et al. reported on similar structured organic transistor-based memory devices, but they used the organic insulator (polymethylmethacrylate (PMMA)) as the gate dielectric layer [54]. Long retention time was reported under a vacuum environment. Kim et al. reported on the use of high-k tunnelling oxide layer (HfO_2) for organic transistor-based nano-floating gate memory devices [55]. A thin HfO_2 tunnelling dielectric layer was found to be good for charge injection as well as data retention. The gold nanoparticles synthesized by the citrate reduction method were adsorbed on the LbL assembled polyelectrolyte layer (PAH/PSS/PAH) via electrostatic interaction. Their group also reported the use of PMMA as the tunnelling dielectric layer (Fig. 7a) [56]. In that case, a very large memory window (~34 V) was obtained (Fig. 7b) and reasonable data retention properties were reported under ambient air conditions. There was a report regarding the use of polymeric materials for both tunnelling and blocking dielectric layers. Zhen et al. reported on the programmable memory characteristics using the device structure of n+Si (gate)/polyimide (PI) blocking dielectric layer/Au_{NP}/PI tunnelling dielectric layer/copper phthalocyanine (CuPc) channel layer/Au source-drain electrodes [57]. The gold nanoparticles were synthesized on the blocking PI layer by e-beam evaporation. Multiple charge trapping layers were reported to be used in organic nano-floating gate memory devices. Kim et al. utilized LbL self-assembled, multilayered gold nanoparticle charge trapping elements for increasing the memory window [58]. Bottom-gate and top-contact structured organic transistor-based memory devices were used as the prototype of memory devices as shown in Fig. 8. The memory window increased from 11 V to 14.6 V by increasing the number of charge trapping layers from 2 to 3 layers. This work is based on the simple solution-processed multi-stack charge trapping layers, so there is a great potential for this technology to be adopted in flexible memory devices with improved programmable memory characteristics. Ryu et al. reported on the use of double-stacked metal nanocrystal layers for non-volatile memory applications [59]. They used different deposition sequences of gold and nickel nanoparticle-charge trapping layers (i.e. Ni/Ni, Au/Au, Ni/Au, and Au/Ni) and found that higher and lower work function metal nanoparticle combinations

Figure 8



Schematic illustration of the organic transistor-based nano-floating gate memory device with layer-by-layer assembled multi-stack charge trapping layers. Figure adopted from ref. [58]. Copyright 2010, IEEE

for top and bottom charge trapping layers (here, Au/Ni combination) could provide fast program/erase speeds as well as long retention times. Another approach to fabricate nano-floating gate memory devices is using 1-dimensional nanostructures (nanotubes or nanowires) for use in the channel layer. Ganguly et al. reported on the fabrication of gold nanoparticle-based non-volatile memory devices using carbon nanotubes (CNT) [60]. The bottom gate (p+Si) and top contact (Au) structured transistor was fabricated with thermal SiO_2 as a gate oxide layer and CNT as the channel layer. On top of the CNT, 5 nm-thick SiO_2 and self-assembled gold nanoparticles were deposited sequentially by electron-beam evaporation. They showed the possibility of multi-level operations of the CNT-based nano-floating gate memory devices by the Coulomb blockade effect. Jeon et al. reported on the use of silicon nanowires as the channel layer with electrostatically assembled gold nanoparticles [61]. The memory device showed a memory window of around 1.5 V. ZnO nanowire is also reported to be used in nano-floating gate memory devices [62]. Colloidal gold nanoparticles were adsorbed onto the Al_2O_3-covered ZnO nanowires and, finally, top gated nanowire-based nano-floating gate memory devices were developed. Low voltage operation was demonstrated and around 1 V of memory window was observed through the static gate bias sweeping. Recently, Kim et al. reported the fabrication of gold nanoparticle-based flexible organic memory devices on plastic substrates at low temperature. From the optimization of device structures they demonstrated good programmable memory characteristics, enhanced device reliability, and good mechanical stability. This device can potentially be applied to advanced flexible electronic devices and integrated organic device circuits [63].

4 Summary and outlook

Extensive research has been performed on the fabrication and characterization of nano-floating gate memory devices based on gold nanoparticles. Gold nanoparticles have been shown to be a promising material for use as the charge trapping element in nanoparticle-based non-volatile memory devices since they are chemically stable and have a high work function. Various device structures as well as operation schemes have been proposed. Also, many strategies have been employed to synthesize gold nanoparticles for the purpose of enhancing the programmable memory characteristics and reliability performances of devices. Now gold nanoparticle-based non-volatile memory devices are fabricated on various substrates, from conventional silicon substrates to flexible substrates, with excellent programmable memory characteristics. However, the research and development of gold nanoparticle-based non-volatile memory devices are still limited to the fabrication and characterization of unit devices. Therefore, the next step is to fabricate integrated non-volatile memory devices using gold nanoparticles for product-level device applications.

Acknowledgements

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About the author

Prof. Jang-Sik Lee received his B.S., M.S., and Ph.D. degrees in materials science and engineering from Seoul National University, Seoul, Korea in 1997, 1999, and 2002, respectively. In 2002, he joined the Los Alamos National Laboratory as a director’s postdoctoral fellow. In 2004, he joined the memory division of Samsung Electronics as a senior research engineer and was in charge of the integration and device reliability of 32 gigabit flash memory devices. Since 2006, he has been with the Kookmin University, Seoul, Korea, where he is currently an assistant professor in the School of Advanced Materials Engineering. He has authored more than 80 research publications and patents. His research interests include non-volatile memory devices (flash, SONOS, nanocrystal devices, FRAM, MRAM, PRAM, ReRAM); low-temperature poly-Si thin film transistors; nanostructured materials and devices; epitaxial thin film growth and applications. He is a member of IEEE, Materials Research Society, Electrochemical Society, and the Korean Institute of Metals and Materials. He is an editor of Electronic Materials Letters and Journal of the Korean Institute of Electrical and Electronic Material Engineers.

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