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CORRECTION TO "VLSI ARRAY PROCESSORS' BLOCK IMPLEMENTATION OF IIR DIGITAL FILTERS" [1]

Vassilis G. Mertzios[2]

In this paper[1] the following corrections should be made:

1. In Figure 4 the second input $v(kL+L)$ should be $v(kL+L-2)$.
2. In (16) and (17) $T_{\mathbf{B}_1}$ should be $T_{\hat{\mathbf{B}}_1}$.
3. Equations (20)-(23) should read as follows:

$$T_f = T_{\hat{\mathbf{B}}_1} + T_{\mathbf{B}_0^{-1}} = N + L, \tag{20}$$

$$F_s \leq \frac{L}{T_f} = \frac{L}{N+L}, \tag{21}$$

$$R = L\frac{1}{\tau T_f} = \frac{L}{(N+L)\tau}, \tag{22}$$

$$\frac{L}{(L+L)\tau} = \frac{1}{2\tau} \leq R < \frac{1}{\tau}. \tag{23}$$

4. The six lines after (23) should be replaced by:

i.e., the lower and upper bounds of magnitude of the throughput rate R are specified by the time τ needed to perform one multiplication and one addition. The increase of L leads to an increase of R. However, the increase of L is actually limited by a number of practical implications which are referred to in the sequel [20]:

[1] V. G. Mertzios and V. L. Syrmos, *Circuits, Systems and Signal Processing*, vol. 7, pp. 79-94, 1988.

[2] Department of Electrical Engineering, School of Engineering, Democritus University of Thrace, 67 100 Xanthi, Greece.