A 1.2 V Low-Noise-Amplifier with Double Feedback for High Gain and Low Noise Figure

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Abstract. In this paper we present a balun low noise amplifier (LNA) in which the gain is boosted using a double feedback structure. The circuit is based in a conventional Balun LNA with noise and distortion cancellation. The LNA is based in two basic stages: common-gate (CG) and common-source (CS). We propose to replace the resistors by active loads, which have two inputs that will be used to provide the feedback (in the CG and CS stages). This proposed methodology will boost the gain and reduce the NF. Simulation results, with a 130 nm CMOS technology, show that the gain is 23.8 dB and the NF is less than 1.8 dB. The total power dissipation is only 5.3(since no extra blocks are required), leading to an FOM of 5.7 mW^{-1} from a nominal 1.2 supply.

Keywords: CMOS LNAs, Noise canceling, Wideband LNA.

1 Introduction

Nowadays, there is a high demand for wireless communications, which includes Industrial, Scientific, and Medical (ISM) and Wireless Medical Telemetry Service (WMTS) applications [1]. These low cost applications require low power, low voltage transceivers fully integrated in a single chip [2-4]. The LNA that is a key block in these systems will be investigated in this paper.

Wideband LNAs with high gain and low noise figure (NF), using noise and distortion cancelation have been proposed [5-7]. But, these circuits have large power dissipation for high gain and low noise figure.

In this paper our main goal is to design a very low area and low cost LNA, with very high gain and low NF using a 1.2 V supply. This is obtained by replacing the load resistors by transistors biased close to saturation. In [7]a circuit operating at 1.2 V with controllable gain was proposed. In this paper we investigate the possibility of introduce a double feedback technique to boost the gain and reduce the noise figure (NF).

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Equations for gain and noise figure are presented, which can be used to optimize the circuit performance. A circuit prototype in a 130 nm standard CMOS technology at 1.2 V have been designed and simulated to demonstrate the proposed technique.

The circuit prototype has gain of 23.8 dB and NF below 2 dB, dissipating only 5.3 mW, leading to a FOM of 5.7 mW^{-1}, which is, to the authors' knowledge, the best FOM in the literature for LNAs with a nominal 1.2 V supply.

2 Contribution for Internet of Things

Recently, more devices are being embedded with sensors and actuators with the ability to communicate and exchange information, creating a cloud environment. The physical communication plays a critical role in portable wireless devices equipped with transceivers where power consumption, immunity to noise, and signal amplification are important parameters to ensure a reliable and efficient communication in a crowded channel environment. With this goal in mind the design of RF front-end blocks for low power applications, in CMOS technology, will contribute towards the achievement of more cheap and robust devices. In this paper we will focus on the design of low power LNAs.

3 Balun LNA with Noise Cancellation

In a receiver path, since typically, the antenna and RF filters are single-ended, it is very important to have a LNA with single-ended configuration input. A differential signal in the receiver is preferred to reduce harmonic distortion and to reject power supply and substrate noise [6]. Traditionally, we have an external balun that converts single-ended signals to differential, but it introduces losses and degrades the receiver NF. A balun LNA is a very good solution to convert a single-ended to a differential signal, which simplifies the design avoiding he external balun [6].

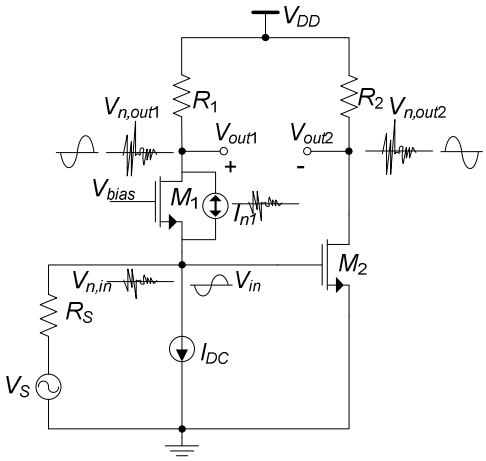


Fig. 1. Balun LNA with noise canceling of CG-transistor [6]

A balun LNA, in which the thermal noise of CG-transistor is canceled because this noise appears in phase at two outputs and their gains are in opposition, is proposed in [6]. The gain is doubled and the noise is reduced when the output signals are balanced. It can also be shown that the distortion introduced by M_1 is also cancelled.

The differential voltage gain of the LNA is obtained from the difference of the common-gate (CG) stage and the common-source (CS) stage gains:

$$A_v|_{Diff} = g_{m1}(R_1//r_{ds1}) + g_{m2}(R_2//r_{ds2}) . \quad (1)$$

where, r_{ds} is the transistors output resistance and g_m is the transconductance.

The input impedance is given, approximately:

$$Z_{in} = \frac{1}{g_{m1}} . \quad (2)$$

Note that the body and source of M_1 are connected to eliminate the body effect.

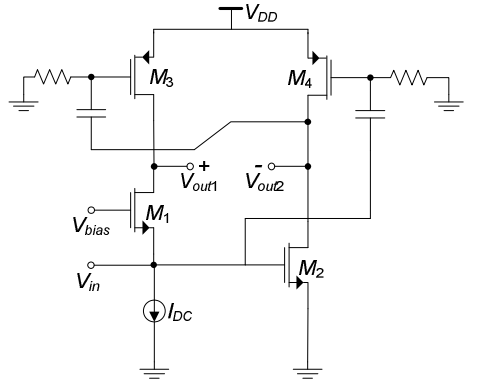
4 Proposed Circuit

Considering the traditional CG-CS LNA circuit (Fig. 1) as reference, we investigate a topology using active loads, by replacing the resistors by transistors, biased in the triode region, which behave, approximately, as linear resistors [7]. In order to enhance the gain, while maintaining a low noise figure, we investigate first the possibility to use local Feedforward and Feedback (FF), as shown in Fig. 2a).

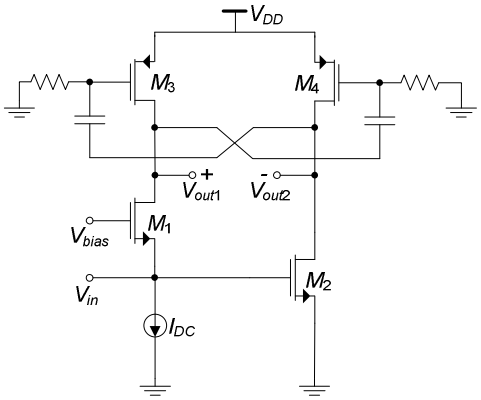
Taking the advantage of using transistors, instead of resistors, we applyV_{in} on the gate of transistor to the gate of M_4, which is amplified and added to V_{out2}. The resulting signal is amplified through $M_3$by feedback and added to V_{out1}. With this structure we have a significant increase in the gain, mainly in the CG stage, which need to be carefully designed to ensure 50 Ohms input match. In this case the thermal noise of M_1 is only partially cancelled, which degrades the LNA noise figure. To overcome this issue we propose a new circuit approach in which we apply a Double Feedback structure (DF), as shown in Fig. 2b).

This proposed circuit boost the gain, and reduce the noise of M_1that appears with the same level on the LNA outputs (load transistors $M_3$and M_4), while the output signals remain balanced. This circuit is more simply and completely symmetrical, and therefore, is expected to achieve the best performance results.

In the feedback is used a high pass RC coupling, as shown in Fig. 2. With these connections, the parasites capacitances of M_3 and M_4 will reduce the bandwidth (the gate-source and gate-drain capacitances), but the main goal is achieved: high gain and low NF.



a)



b)

Fig. 2. a) LNA using FF. **b)** Proposed LNA using DF

In order to provide some circuit insight, we derive here the equations for gain (CG and CS stages) and LNA input impedance (for the proposed DF case):

$$\frac{V_{out1}}{V_{in}} = \frac{g_{mCG}g_2 + g_{m2}g_{m3}}{g_1g_2 - g_{m3}g_{m4}} . \tag{3}$$

$$\frac{V_{out2}}{V_{in}} = -\frac{g_{m2}g_1 + g_{mCG}g_{m4}}{g_1g_2 - g_{m3}g_{m4}} . \tag{4}$$

where,

$$g_1 = g_{ds1} + g_{ds3} .$$

$$g_2 = g_{ds2} + g_{ds4} .$$

Using (3) and (4), we obtain the LNA differential gain,

$$A_v|_{Diff} = \frac{V_{out1}-V_{out2}}{V_{in}} = \frac{g_{mCG}(g_{m4}+g_2)+g_{m2}(g_{m3}+g_1)}{g_1 g_2 - g_{m3}g_{m4}} . \quad (5)$$

The input-impedance is given by

$$Z_{in} = \frac{g_1 g_2 - g_{m3}g_{m4}}{g_{mCG}[g_2 g_{ds3} - g_{m3}g_{m4}] - g_{m2}g_{m3}g_{ds1}} . \quad (6)$$

Using equations (5) and (6), we can optimize the circuit performance in order to increase the gain, minimizing the impact in the input match.

From [6, 7], if it is assumed that $g_{m1} = g_{m2} = g_m$, the noise factor is:

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S c_{ox} f^{\alpha f}}\left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2}\right) + \frac{\gamma}{2R_S g_m} + \frac{1}{R_S r_{ds} g_m^2} . \quad (7)$$

where k is Boltzmann's constant, c_{ox} is the oxide gate capacitance per unit area, W_i and L_i are the transistor dimensions, T is the absolute temperature, γ is the excess noise factor, k_f and α_f are intrinsic process parameters, which depend on the size of the transistors [8, 9]. With the proposed circuit there is additional noise due to the double feedback structure, however, this can be minimized by proper design.

From [6], to improve the noise figure, the g_{m2} should be greater than g_{m1}, while the g_{ds4} is increased to keep the output signals balanced.

$$g_{m2} = n \cdot g_{m1} .$$

$$g_{ds4} = n \cdot g_{ds3} .$$

The optimal value of *n* is obtained by simulations.

5 Simulation Results

The circuit prototype is designed using a $130\,nm$ CMOS standard technology with $1.2\,V$ supply. The circuit parameters are given on Table 1. The length of each transistor channel is the minimum to maximize speed, and V_{bias} is defined in $760\,mV$ to define the biasing current at the CS stage.

Table 1. LNA circuit parameters using DF

	I_D (mA)	W (μm)	r_{ds} (Ω)	g_{ds} (mS)	g_m (mS)
M_1	2	139.2	472	2.12	30.80
M_2	2.43	358.4	357	2.80	44.23
M_3	2	13.14	236	4.23	2.07
M_4	2.43	16.4	186	5.38	2.48

In Table 2 we compare the theoretical results with simulations. We use equation (1) to traditional LNA with resistors[6] and using MOS in triode [7], and equation (5) for the proposed DF approach.

Table 2. Gain (dB) for different topologies

	Res	*MOS*	*DF*
Theoretical	19.07	20.45	23.78
Simulation	19.03	20.50	23.81

In Table 3 we compare the simulation results for the traditional case with resistors, MOS transistors, and two approaches capable to boost the gain: 1) using feedback and feedforward (FF), and 2) the proposed case of double feedback (DF).

In order to investigate the influence of double feedforward in the LNA key parameters: gain, noise figure, linearity, and frequency band, several simulations are presented in Table 3. For a better comparison of the obtained results, the following figure of merit is used [10]:

$$\mathrm{FOM}[\mathrm{mW}^{-1}] = \frac{Gain}{(NF-1)P_{DC}[\mathrm{mW}]}. \tag{8}$$

Table 3. Circuit Simulations for different topologies

	$Gain$ (dB)	NF (dB)	$IIP3$ (dBm)	$Power$ (mW)	$Band$ (GHz)	FOM (mW^{-1})
Res	19.03	< 2.34	3.62	5.16	0.2-7.4	2.43
MOS	20.50	< 2.02	-3.47	5.30	0.2-6	3.37
FF	23.28	< 2.39	-11.03	5.51	0.1-2.5	3.61
DF	23.81	< 1.79	-9.92	5.32	0.1-2	5.72

In Table 3 is shown that the DF approach has the highest gain and the lower NF, leading to the highest FOM. The disadvantages are the increase of the circuit non-linearity and the reduction of the available bandwidth.

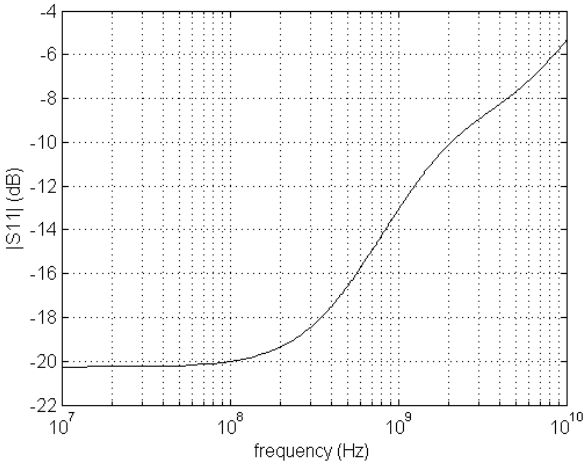


Fig. 3. Simulated LNA S11 parameter

In figs. 3 to 5, the simulation results for the input match (S11), gain, and NF, for the proposed circuit (DF) are presented.

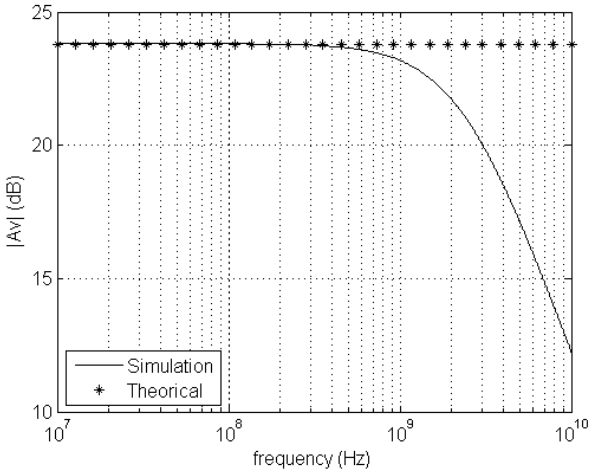


Fig. 4. Simulated LNA Gain

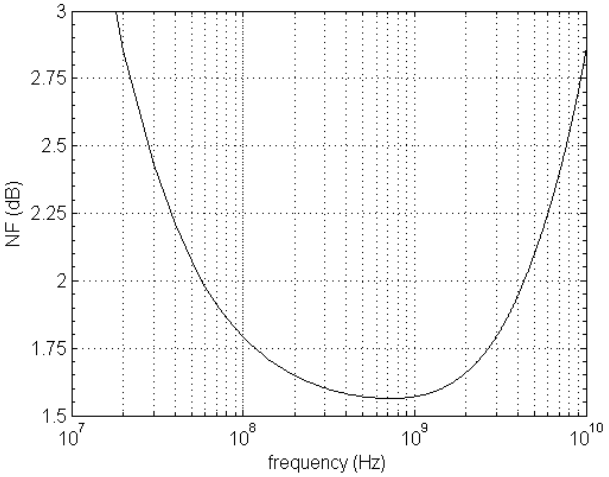


Fig. 5. Simulated LNA Noise Figure

Comparing these results with state-of the art inductorless LNA (table4),we observe that our circuit is very good in terms of gain and NF, and has very low power, which leads to the best FOM (please note that the results are obtained by simulation, some degradation is to be expected in the fabricated circuit; some of the references in table 4 are from measurements).

Table 4. Comparison with state-of-the art LNAs

Ref	Tech (nm)	Band (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	FOM (mW^{-1})
[6]^{M}	65	0.2-5.2	13-15.6	< 3.5	>0	14	0.4
[11]^{M}	90	0.5-8.2	22-25	< 2.6	-4/-16	42	0.5
[12]^{M}	90	0.8-6	18-20	< 3.5	>-3.5	12.5	0.6
[13]^{S}	90	0.1-1.9	20.6	< 2.7	10.8	9.6	1.3
[14]^{S}	130	0.2-3.8	11.2	< 2.8	-2.7	1.9	2.1
[15]^{M}	180	0.5-0.9	16	< 4.3	-	22	0.2
[16]^{M}	180	0.1-0.9	15	< 4.2	-	10	0.3
[7]^{S}	130	0.2-5	20.4	2.6	-10.9	4.8	2.7
[17]^{S}	130	0.2-6.6	19.8	< 1.8	1.6	4.8	3.5
This Work^{S}	**130**	**0.1-2**	**21.7-23.8**	**1.6-1.8**	**-9.7**	**5.3**	**5.7**

(^{S}) - Simulation results. (^{M}) - Measurement results.

The proposed circuit approach is especially interesting in low power and low voltage biomedical applications [1]. Since in these applications low power is the key aspect and some non-linearity can be tolerated. There are ISM bands in 450 MHz and 900 MHz and WMTS band in 600 MHz and 1.4 GHz, for which this circuit can be a good alternative to the conventional solutions.

6 Conclusions

In this paper we present a low voltage and low power wideband balun LNA with DF for high gain and low NF. A circuit prototype operating at 1.2 V is presented in a 130 nm CMOS technology, which validates the proposed methodology. Simulation results show that the gain of the balun LNA is 23.8 dB, and the NF is below 2 dB for a power consumption of 5.3 mW. The proposed circuit is especially useful for low power and low voltage operation in biomedical applications (ISM and WMTS bands).

The proposed circuit, with 1.2 V supply, to the best of the authors' knowledge, has the high FOM (5.7 mW^{-1}) when compared with CMOS LNAs in the literature.

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