

# Enhancing a Layout-Aware Synthesis Methodology for Analog ICs by Embedding Statistical Knowledge into the Evolutionary Optimization Kernel

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**Abstract.** This paper applies to the scientific area of electronic design automation (EDA) and addresses the automatic sizing of analog integrated circuits (ICs). Particularly, this work presents an innovative approach to enhance a state-of-the-art layout-aware circuit-level optimizer (GENOM-POF), by embedding statistical knowledge from an automatically generated gradient model into the multi-objective multi-constraint optimization kernel based on the NSGA-II algorithm. The approach was validated with typical analog circuit structures, using the UMC 0.13  $\mu\text{m}$  integration technology, showing that, by enhancing the circuit sizing optimization kernel with the gradient model, the optimal solutions are achieved, considerably, faster and with identical or superior accuracy. Finally, the results are Pareto Optimal Fronts (POFs), which consist of a set of fully compliant sizing solutions, allowing the designer to explore the different trade-offs of the solution space, both through the achieved device sizes, or the respective layout solutions.

**Keywords:** Analog Integrated Circuits Design, Automatic Sizing, Electronic Design Automation, Evolutionary Computation, Gradient Model.

## 1 Introduction

In the System-on-Chip (SoC) age it is common to find devices where the whole system is integrated in a single chip, this is done to reduce production costs and increase performance. These complex integrated circuit (IC) designs are established in telecommunications, medical and multimedia applications, where blocks of Analog and Mixed-Signal (AMS), digital processors and memory blocks appear together [1]. Presently most functions in mixed-signal ICs and SoC designs are implemented using digital or digital signal processing (DSP) circuitry, where analog blocks constitute only a small part of the components, being essentially the link between digital circuitry and the continuous-valued external world. However, when integrating digital and analog circuits together on the same die, it becomes notorious that the development time of analog blocks is much higher when compared to the digital counterpart [2]. This difference is due to that analog design in general is less

systematic, more heuristic and knowledge intensive than digital, and the lack of maturity of the EDA that are in fact used by analog designers.

Historically, the tools for automated circuit sizing are classified as knowledge-based or optimization based, and an extensive analysis of the related work can be found in [1]. The early strategies [5] tried to systematize the design by using a pre-designed plan built with equations and a design strategy provided by the designer, which will produce component sizes that meet the performance requirements. Despite the short execution time, deriving the design plan is hard and time-consuming, and it requires constant maintenance in order to keep it up to date with technological evolution, also, the results are not optimal, suitable only as a first-cut-design.

Aiming for optimality, the next generations of sizing tools apply optimization techniques. Based on the evaluation techniques employed, the optimization-based sizing tools can be further classified into two main sub-classes, respectively, equation-based and simulation-based. The equation-based approaches [6][7] use analytic design equations to evaluate the circuit's performance during the optimization loop. The main drawbacks are that not all design characteristics can be easily mapped by analytic equations and the approximations introduced in the equations yield low accuracy designs, suited only to derive first-cut designs. The simulation-based approaches [8] [9] [10] use an electrical simulator to evaluate the circuit's performance. The strong points of this approach are generality and easy-and-accurate model, however, typified by long execution time. In order to cope with this limitation alternative approaches have been explored, e.g., use equations to derive an approximate initial solution, use parallel mechanisms that shares the evaluation load among multiple computers, use macro modeling techniques to speed up the evaluation of the circuit's performance, etc.

In this paper, a methodology to enhance the state-of-the-art layout-aware circuit-level optimizer, GENOM-POF [3], by adding circuit specific knowledge that is automatically extracted using machine learning techniques is described. The Gradient Model, here introduced, is embedded in the genetic operators of the NSGA-II [4] optimization kernel and is generated by sampling the design space, extracting and ranking the contributions of each design variable to each performance measure or objective, and, finally, building the model based on a set of gradient rules.

This paper is organized as follows: next section briefly highlights the contributions to technological innovation; then, in section 3, the enhanced GENOM-POF with Gradient Model is described; afterwards, in section 4, the achieved results are discussed; and finally, in section 5, the conclusions are presented.

## 2 Contribution to Internet of Things

The implementation of Internet of Things requires low power circuits using challenging integration technologies. The design of such circuits includes the design of analog-to-digital and digital-to-analog interfaces which are highly specialized and time consuming, even for expert designers. The electronic design automation is a fundamental research area supporting the designer to find optimal implementation solutions in a reduced time frame.

### 3 GENOM-POF Enhanced with the Gradient Model

GENOM-POF is part of the AIDA [11], an analog IC design automation framework that results from the integration of two in-house tools, GENOM-POF, and, LAYGENII [12], that performs the automatic layout generation from circuit-level specifications. Before moving to the description of how the gradient model is used to enhance GENOM-POF, the tool is reviewed and contextualized.

#### 3.1 GENOM-POF Architecture

GENOM-POF is based on the elitist multi-objective evolutionary optimization kernel NSGA-II, and uses the industrial grade simulator HSPICE® to evaluate the performance of the design. It targets the design of robust circuits, by allowing the consideration of corner cases during optimization.

The inputs are the circuit and test-benches in the form of HSPICE® netlists, and the layout template required by LAYGEN II to instantly generate the floor plan of each of the sizing solutions. The designer also defines ranges for the optimization variables, design constraints, and optimization objectives. Then, GENOM-POF models the circuit as an optimization problem, defined by the tuple  $\{x - \text{optimization variables}, F(x) - \text{objective functions}, G(x) - \text{constraint functions}\}$  and suitable to be optimized by the NSGA-II kernel. The output is a family of Pareto optimal sized circuits that fulfill all the constraints and represent the feasible tradeoffs between the different optimization objectives.

In this work, the gradient model is integrated in GENOM-POF by embedding the extracted circuit knowledge into the evolutionary kernel operators increasing their efficiency. The enhanced GENOM-POF architecture is shown in Fig. 1, and the next section describes in detail how the integration is performed.

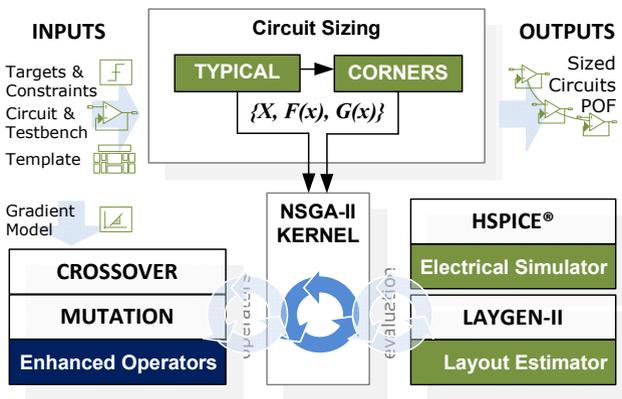


Fig. 1. GENOM-POF architecture with the integration of the Gradient Model

### 3.2 Gradient Model Generation

The automatic generation of the Gradient Model is based on the Design of Experiments (DOE) [13] technique to sample the circuit behavior. The gradient model is generated by sampling the circuit design space (using DOE), extracting and ranking the contributions of each design variable (input) to each design performance or objective (output), and finally, building a set of gradient rules that will be used to enhance GENOM-POF. Two approaches of DOE will be used in this work, full factorial design and fractional factorial design. The number of samples, electrical simulations, required to construct the DOE's matrix (or just matrix), of both strategies obeys to the following equation:

$$\text{Number of simulations} = B^{(n-p)} \quad (1)$$

where  $B$  is the number of points per variable or matrix base ( $B > 1$ ),  $n$  is the number of input variables and  $p$  the number of non-elementary input variables. In the full fractional DOE the circuit is sampled in all the combinations of variables' values. For each variable ( $x_i$ ),  $B$  logic levels are defined, and to each value, it is assigned a value  $v_{i,b}$  derived from the variable's range according to eq. 2.

$$v_{i,b} = X_i^{Min} + \frac{(X_i^{Max} - X_i^{Min})}{2B} \times (1 + 2b), \quad b = 0, \dots, B - 1 \quad (2)$$

The next step is to perform the statistical analysis of the experiments in order to understand which variables affect most the outputs; this is called the main effect. The main effect is the effect of one independent (input) variable on the dependent (output) variable, ignoring the effects of all other independent variables, where  $m_{i,j}$ , the main effect of input variable  $i$  in the output variable  $j$  is computed according to eq. 3.

$$m_{i,j} = \sum_{k=1}^{B^{n-p}} w_{i,k} \times y_k, \quad w_{i,k} = \begin{cases} +1 & \text{when } x_{i,k} \geq B/2 \\ -1 & \text{when } x_{i,k} < B/2 \end{cases} \quad (3)$$

where  $k$  identifies the sample and  $y$  the output measure for the sample. When the total main effect of an input variable is positive/negative, this is an indication that if the value of that input variable is increased, the value of the output will tend to increase/decrease.

Then, a refinement procedure is executed. For each output variable  $y_j$ , a new DOE matrix is constructed using the fractional factorial sampling, with the  $N$  input variables that have the larger contributions as the only elementary variables.

The refined DOE matrix is then converted to the set of gradient rules for that output variable. This is done by discarding the columns referring to non-elementary variables and transforming the levels of the elementary variables  $x_i$  into input gradient symbols  $Si_{i,j,k}$  according to:

$$Si_{i,j,k} = \begin{cases} (+) & \text{when } x_{i,k} \geq B/2 \\ (-) & \text{when } x_{i,k} < B/2 \end{cases} \quad (4)$$

where  $k$  identifies the line of the matrix. The output gradient symbols  $So$  are converted from the output values as:

$$So_{j,k} = \begin{cases} (+) & \text{when } y_{j,k} \geq Y_j^{Max} - \Delta_j \\ (U) & \text{when } (Y_j^{Min} + \Delta_j) < y_{j,k} < (Y_j^{Max} - \Delta_j) \\ (-) & \text{when } y_{j,k} \leq Y_j^{Min} + \Delta_j \end{cases} \quad (5)$$

where  $Y_j^{Max}$  and  $Y_j^{Min}$  are, respectively, the maximum and minimum values of the output  $y_j$  obtained in the DOE matrix (not the refined DOE matrix), and  $\Delta_j$  is  $|Y_j^{Max} - Y_j^{Min}|/3$ . The meanings of the symbols are: (-) decrease; (+) increase and (U) undefined.

### 3.3 Gradient Model applied to the Mutation Operator

The integration of the Gradient Model into GENOM-POF is done in two fronts, first by embedding it in the evolutionary operator of mutation and second by adding the Gradient Model setup interface to the AIDA graphical user interface.

In GENOM-POF the chromosome is represented by the vector of continuous variables  $= \{x_1, \dots, x_n\}$  representing the design variables. In order to speed up the convergence of the algorithm the gradient model is used to introduce design knowledge into the mutation operator.

The mutation operator in GENOM-POF uses the continuous valued operator introduced Deb and Goyal in [4]. In this operator,  $\delta_i$  defined as  $\delta_i = (x_i^M - x_i)/(X_i^{Max} - X_i^{Min})$ , where  $x_i^M$  and  $x_i$  are the mutated and original values respectively, is the mutation perturbation applied.  $\delta_i$  is a random variable, with values in  $[-1, 1]$  and *p.d.f.*

$$P(\delta) = 0.5 \times (\eta + 1) \times (1 - |\delta|)^\eta \quad (6)$$

A factor of disturbance  $\bar{\delta}$  of  $\delta$  can be obtained from an uniform random number  $u \in [0, 1[$  using eq. 6, which is obtained from eq. 7 by solving  $\int_{-1}^{\bar{\delta}} P(\delta) = u$ .

$$\bar{\delta} = \begin{cases} (2u)^{\frac{1}{\eta+1}} - 1, & \text{if } u < 0.5 \\ 1 - [2(1-u)]^{\frac{1}{\eta+1}}, & \text{if } u \geq 0.5 \end{cases} \quad (7)$$

The mutated value,  $x_i^M$ , is given by  $x_i^M = x_i + \bar{\delta}_i(X_i^{Max} - X_i^{Min})$ . The gradient rules are then applied. The application of the rules follows the expression in eq. 8:

$$x_i^G = (1 + \mu \cdot \gamma(Si_i))x_i^M \quad (8)$$

where  $x_i^G$  is the variable value after the application of the rule,  $\gamma(Si_i)$  is a function of the gradient symbol defined in eq. 9, and  $u \in [0, c[$  is a uniformly distributed random number between 0 and  $c$ , the change rate model parameter.

$$\gamma(Si_i) = \begin{cases} +1 & \text{when } Si_i = (+) \\ -1 & \text{when } Si_i = (-) \end{cases} \quad (9)$$

The rules are selected by searching for each optimization objective if there is a rule that causes the desired effect in the corresponding response variable. Finally, fig. 2 illustrates how the automatic generated gradient model is applied to the mutation operator.

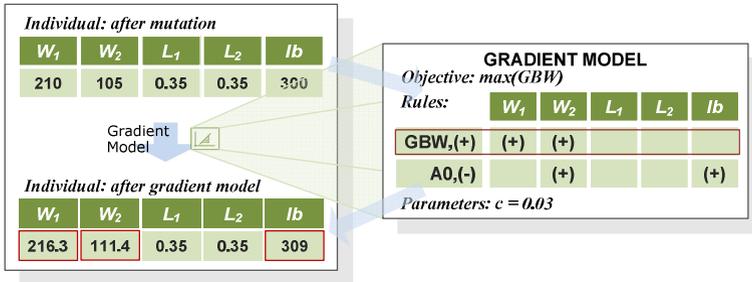


Fig. 2. Example of applying the Gradient Model to the mutation operator

## 4 Results

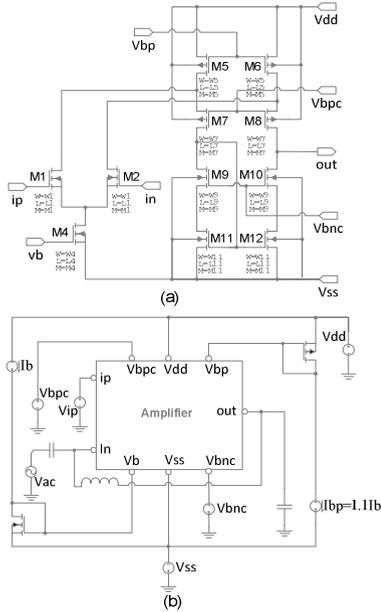
The proposed methodology was tested on an Intel® Core™ 2 Quad CPU 2.4 GHz with 6 GB of RAM and multi-threads to perform the evaluation process of each population.

The circuit used to compare the GENOM-POF with GENOM-POF integrated with Gradient Model is the single ended folded cascade amplifier, presented in Fig. 3(a)(b). For the setup of this comparison the items required were the net list and the test bench of the circuit. This case study was done considering 15 input variables, 2 objectives and 19 constraints defined in Fig. 3(c). The optimization variables are the widths and lengths of the cascade bias tensions  $vbnc$  and  $vbp_c$ , and the bias current. This circuit is optimized in both GENOM-POF and GENOM-POF integrated with Gradient Model in exactly the same conditions, for a fair comparison. For this study all the 15 input variables are considered, the Gradient Model was generated with a base of two ( $B = 2$ ) and considering only the design variable with larger contribution ( $N = 1$ ). The extracted gradient rules for the optimization objective are shown in Fig. 3(d). The model was automatically generated in less than 5 minutes and can be reused.

Fig. 4 illustrates the improvements achieved by the proposed approach. Particularly, it shows that the Gradient Model enhanced GENOM-POF by achieving better solutions at generation 2.000 than GENOM-POF at generation 2.000 or 4.000.

The Fig. 4 also shows that even for 60.000 generations GENOM-POF does not reach the maximum DC Gain obtained by the new approach.

In order to confirm that this is not an isolated case, 20 executions with different seeds were done. The output is shown in Fig. 5, where it can be seen that the inclusion of gradient model consistently lead to better solutions. The 20 runs show an average number of points in the final POF of 51.55 for GENOM-POF and 81.70 for GENOM-POF integrated with Gradient Model. Furthermore, the normalized non-dominated area, which measures the ratio between the non-dominated and dominated area in the performance planer each an average area of 0.43 for GENOM-POF and 0.20 for GENOM-POF integrated with Gradient Model. This confirms the analysis of Fig. 5, where the GENOM-POF enhanced with the Gradient Model produces more and better solutions.



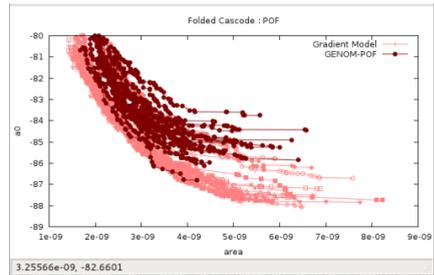
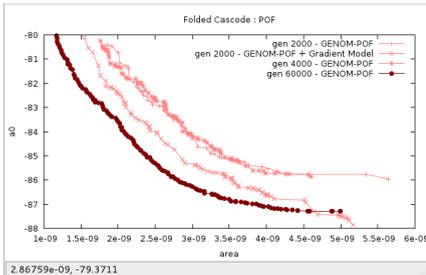
Variables	cn, cp, l1, l4, l5, l7, l9, l11, ib, w1, w4, w5, w7, w9, w11
Ranges	0.18e-6 <= l* <= 5.0e-6 0.24e-6 <= w* <= 200.0e-6 -0.4 <= cn <= 0.0 0.0 <= cp <= 0.4 30.0e-6 <= ib <= 400.0e-6
Objectives	min(area) max(a0)
Constraints	gb >= 1.2e7 a0 >= 80 55 <= pm <= 90 sr >= 1e7 ov_m(*) >= 30e-3 d_m(*) >= 1.2 osp >= 0.3 osn <= -0.3 (* the constraint applies to: M1, M4, M5, M7, M9 and M11)

(c)

Target	Variable / Gradient
A0, (-)	L9, (-)
A0, (+)	L9, (+)
area, (-)	W11, (-)
area, (+)	W11, (+)

(d)

**Fig. 3.** (a) Electrical schematic and (b) testbench of the single-ended folded cascode amplifier and (c) ranges, objectives and constraints. (d) Gradient Rules.



**Fig. 4.** Pareto Fronts: GENOM-POF (for 60,000, 4,000 and 2,000 generations) vs. Enhanced GENOM-POF (for 2,000 generations)

**Fig. 5.** GENOM-POF vs. Enhanced GENOM-POF for 20 different initial populations (for 2,000 generations)

## 5 Conclusions

The work presented in this paper corresponds to an innovative IC design automation approach by embedding a simple but effective design knowledge model, Gradient Model,

into the evolutionary optimization kernel of a state-of-the-art sizing tool. The new technique proved to be capable to accelerate and reduce the execution time of the circuit-level optimizer GENOM-POF. This integration of the Gradient Model with GENOM-POF enhances the optimizer efficiency, forwarding the data to the desired objectives and causing a significant reduction in the number of electrical simulations. The model potential has been proved through a complex case study presented. Finally, the proposed objectives for this work were achieved and a new optimizer was created.

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