Modeling of Syllogisms in Analog Hardware

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Abstract. Syllogistic reasoning is modeled in analog hardware and some hardware models, i.e. syllogisms *Baroco* and *Darii* are presented. Chaining of syllogisms is modeled by using original *min-max entities* (circuits), "to see" whether the two rules, modeled in dedicated hardware, i.e., IF *A* THEN *B* and IF *B* THEN *C* imply the "hardware" rule IF *A* THEN *C*. The preliminaries include original *min-max circuits* based on operational amplifiers (Op-Amp), straight lines Op-Amp generators and different test circuits designed in Electronics WorkBench simulation environment and in real hardware. The "stage" to perform modeling is the phase plane.

Keywords: modeling syllogisms, analog hardware, min-max entities.

1 Introduction

In AI community, the *thinking rational approach* [1] deals with searching for ideal thinking and reasoning methods to provide means for indisputable and efficient problem solving. The thinking rational approach can be expressed by using syllogisms. The aim of this approach is to build systems that are able to solve problems correctly and ideally in the most satisfactory manner regardless of whether humans follow the same reasoning processes. Logicians amongst the AI researchers use the thinking rational approach to design and develop intelligent systems. In this paper, we will use our original min-max-Op-Amp technique approach to model syllogisms in hardware environment. Min-max-Op-Amp technique is based on an idea that *min* and *max* circuits can be designed by using Op-Amp. On the other hand, if we accept an inverting or non-inverting Op-Amp circuit as a straight-line generator in the phase plane (PP) then any kind of transfer function can be synthesized by using *min*, *max*, and Op-Amp circuits. All presented models are realized in Electronics Workbench (commercial software) environment as well as in a real hardware (not shown in the paper). Syllogistic reasoning with min-max-Op-amp technique approach, where the consequence of a rule in one reasoning stage is passed to the next stage as a fact, is essential in building up a large-scale system with high-level intelligence. Already the very first computable AI systems were based on logical reasoning in this sense and many recent developments were initiated or established/advanced by AI scientists (Fuzzy Logic, Default Logic, BDI Logics, etc.).

The thinking rational approach has its origin in philosophy and draws mainly on philosophy and mathematics. The roots of the thinking rational approach are strongly related to the fundamental philosophical problem of "right thinking" which deals with determining how humans could and should reason in order to obtain optimal results. The Greek philosopher Aristotle tried to identify what he called "laws of thought" as foundations of rational thinking. He formulated an informal system of *syllogisms* for the representation of and the deductive reasoning with knowledge [2]. The most famous example of such a syllogism is the argument: "Socrates is a man. All men are mortal. Therefore, Socrates is mortal". It is an example of the most fundamental syllogism; the "syllogism of the first mood of the first figure" to which the other syllogisms are reducible:

All *S* are *M*.
All *M* are *P*.
Therefore, all *S* are *P*.

Such syllogisms as "laws of thought" were designed to deduce correct conclusions from given correct premises (i.e. any conclusions drawn from reasoning with these laws should be indisputable, which means not capable of being proven wrong). The laws of thought were assumed to describe the logical reasoning processes of the rational mind and therefore, the laws of thought are considered as origin of research in logic and logical reasoning. These philosophical roots of this approach are the reason why this approach is also called the *laws of thought approach*.

In the two valued propositional calculus, the chaining syllogism

$$(p \rightarrow q) \wedge (q \rightarrow r) \rightarrow (p \rightarrow r)$$

where p, q, and r are propositional variables, is a tautology, i.e. a formula that is true in every possible interpretation. The chaining rule is one of the most important deduction schemes from a theoretical and practical point of view. It allows combining min-max (fuzzy) IF-THEN rules and because of that reduces the complexity of expert systems [3].

The presentation concept of this paper is figure rich one; "a figure says more than a 1000 words".

Modeling syllogism in analog hardware environment is based on some preliminaries that are described in the second section. In that section, straight-line generators and original min-max circuits based on Op-Amp-technique as well as set test circuits are briefly described. Among logic figures and their valid moods we have chosen Figure I (*Darii*) and Figure II (*Baroco*) to be modeled in analog hardware environment. These models are presented in the third section. In the same section, the simplest way to interpret "hardware deduction", i.e. conclusion is shown.

2   Preliminaries: Min-Max Hardware Circuits (Op-Amp Technique)

Hardware circuit modeling of syllogisms is based on a special class of hardware circuits that have their theoretical stand in mathematical environment of max and min algebra [4]. Min and max circuits "go" with straight-line generators to generate set environment.

Straight-Line Generators. The straight lines can be generated in two ways:

- by using standard operational amplifiers that support the modeling of the expression $l \equiv y = kx + l$ (*Op-Amp-technique*),
- by using EWB component called „Three-Way Voltage Summer" (TWVS straight lines modeling)

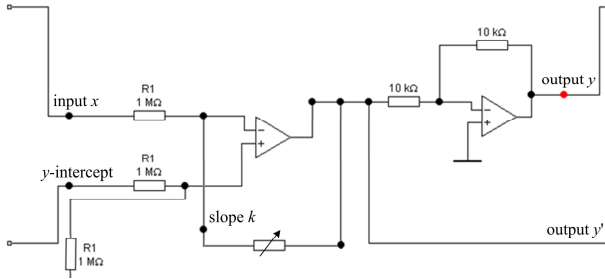as illustrated with schematics shown in Fig. 1 and 2 respectively.

Fig. 1. Hardware model of a straight-line generator based on Op-Amp-technique. Transfer characteristic of a two-stage amplifier represents a straight line in PP.
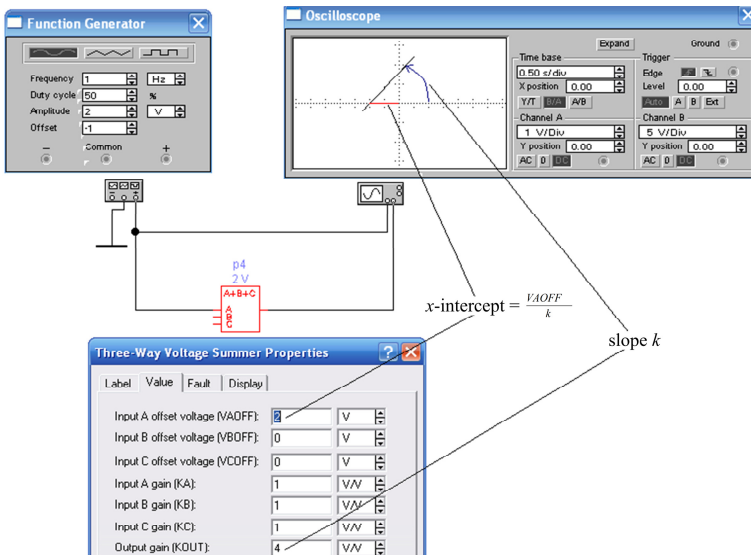
Fig. 2. TWVS straight-line modeling: non-inverting Op-Amp generates a straight line in the PP

Min Circuit. Properties of *min-circuit* operations can be described with the following rule [5]:

If A and B are two subsets of X then their intersection is subset D of X marked as D = A ∩ B such as that for every x∈ X is valid:

$$D(x) = \min[A(x), B(x)] = A(x) \cap B(x) \tag{1}$$

Min operation can be expressed in algebraic form as:

$$\min(a,b) = \big((a+b) - |a-b|\big)/2 \tag{2}$$

Equation (2) defines the (obvious) design of the min circuit; two instrumentation amplifiers are used along with an absolute values circuit (see Fig. 3) [6].
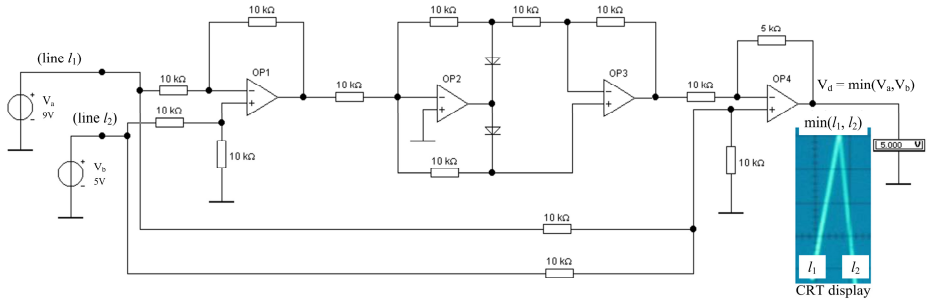
Fig. 3. Min circuit in Op-Amp-technique and its "DC" and "AC" response; Op-Amps are used as generators of straight lines l_1 and l_2

Max Circuit. Properties of *max-circuit* operations can be described with the following rule [5]:

If A and B are two subsets of X then their intersection is subset C of X marked as $C = A \cap B$ such as that for every $x \in X$ is valid:

$$C(x) = \max[A(x), B(x)] = A(x) \cup B(x) \tag{3}$$

Max operation can be expressed in algebraic form as:

$$\max(a,b) = \big[(a+b) + |a-b|\big]/2 \tag{4}$$

By using equation (4), we have designed *max-circuit* in Op-Amp-technique as it is shown with the schematics in Fig. 4 [6].
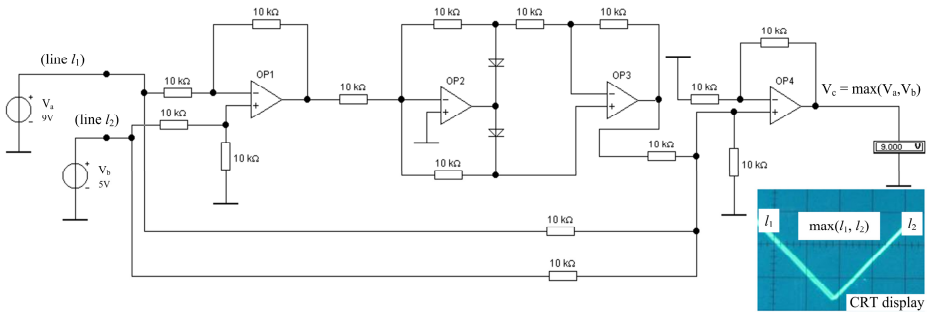
Fig. 4. Max circuit in Op-Amp-technique and its "DC" and "AC" response

Set Test Circuits. There are three different electronic set test circuits to check whether the test point P_T is an element of the solution space (a part of the phase plane).

In the first case, Op-Amp (LM741) is used as a sensing comparator. When the test point lies inside the solution area both comparators will respond (output voltage) with + voltage level turning the AND-gate on. Indicator glows [7].

Action algorithms for all three test circuits are shown along corresponding schematics (see Fig. 5, 6, and 7 respectively).
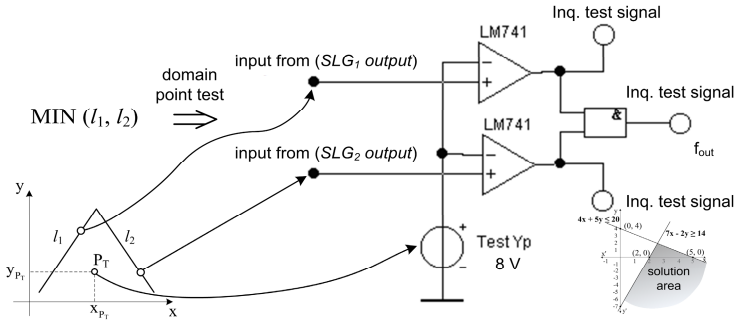
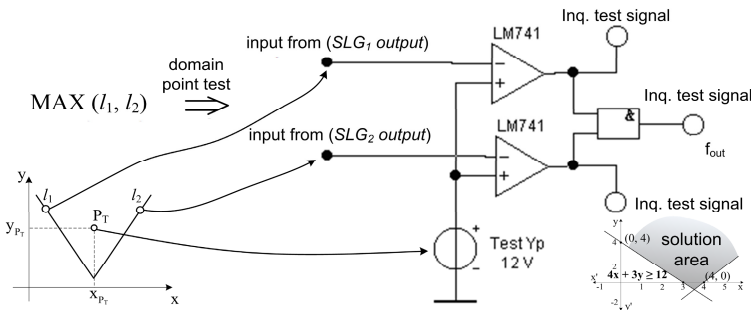**Fig. 5.** $f_{out} = \begin{cases} 1 & if \quad P_T \in MIN\left(L_1, L_2\right) \\ 0 & else \end{cases}$

Fig. 6. $f_{out} = \begin{cases} 1 & if \quad P_T \in MAX\left(L_1, L_2\right) \\ 0 & else \end{cases}$
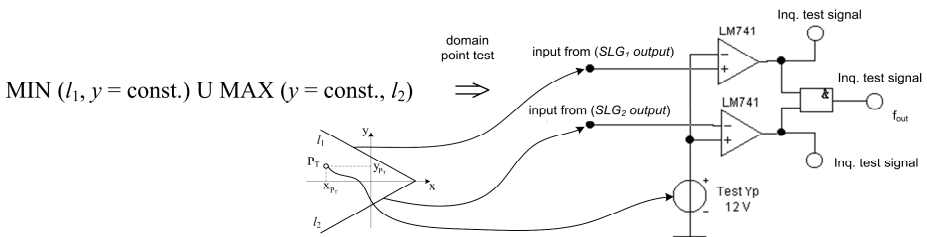
Fig. 7. $f_{out} = \begin{cases} 1 & if \quad P_T \in MIN\left(L_1, y = const\right) \vee MAX\left(y = const, L_2\right) \\ 0 & else \end{cases}$

All of the mentioned set test circuits can be used for testing hardware models of syllogisms, i.e. whether the certain point P_T belongs to a chosen set, or not.
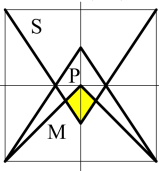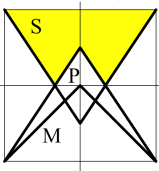
3   Logic Figures Modeling

Indirect deductive rule often appears in the form of categorical syllogism that can be presented with this scheme [8]:

$$M \quad P$$
$$\underline{S \quad M}$$
$$S \quad P$$

where minor term is denoted with letter *S*, major term with letter *P*, and the middle term with the letter *M*. There are four different figures of categorical syllogism, depending on the position of the middle term in the premises (*M   P*, respectively *S M*) [8]. Each of the figures consists of several moods; in the first figure, there are four, in the second, there are also four, in the third, there are six, and in the fourth, there are five. First two figures and their moods are shown in Table 1.

Table 1. Logic figures and their min-max interpretation diagrams

	Figure I	Figure II	I Darii	II Baroco
Major premise	*M P*	*P M*	$M \setminus \min(M,S)$	$\max(S, M, P)$
Minor premise	*S M*	*S M*		
Valid moods	*Barbara Darii* *Darii Ferio*	*Baroco Cesare* *Camestres Festino*		

In this paper, valid moods of categorical syllogisms *Baroco* and *Darii* will be modeled with analog hardware circuits (min-max entities) in order to show that there is a possibility to process indirect deductive rules in analog hardware environment.

Specification of the algorithm for solving syllogisms with min-max entities requires strategies for:

- choosing premises representations,
- unifying premises representations,
- deciding whether there are valid conclusions,
- formulating valid conclusions.

The following example will illustrate the method. Fig. 8 illustrates the method applied to the syllogism *All P are M. Some S are not M*. Each premise is first represented by the diagram of its maximal model, i.e. the one containing the most types of individuals consistent with the premise. Within these diagrams, sub-regions representing the minimal models of the premise are marked with an "*x*". The two

premise diagrams then have to be "registered" which means their *M* entity superimposed and their *P* and *S* entities arranged to form the maximal model consistent with each premise. If their region is bisected by the third entity when the premise diagrams are registered, then the *x* is removed. This ensures that the remaining *x* still mark the minimal models of the conjunction of the two premises.
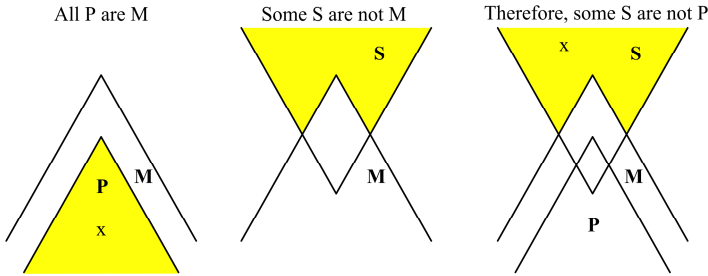

Fig. 8. Min-max entities graphical algorithm applied to the syllogism *All P are M. Some S are not M*.

Figure *Baroco* can be modeled in analog hardware (as it is shown in Fig. 9):

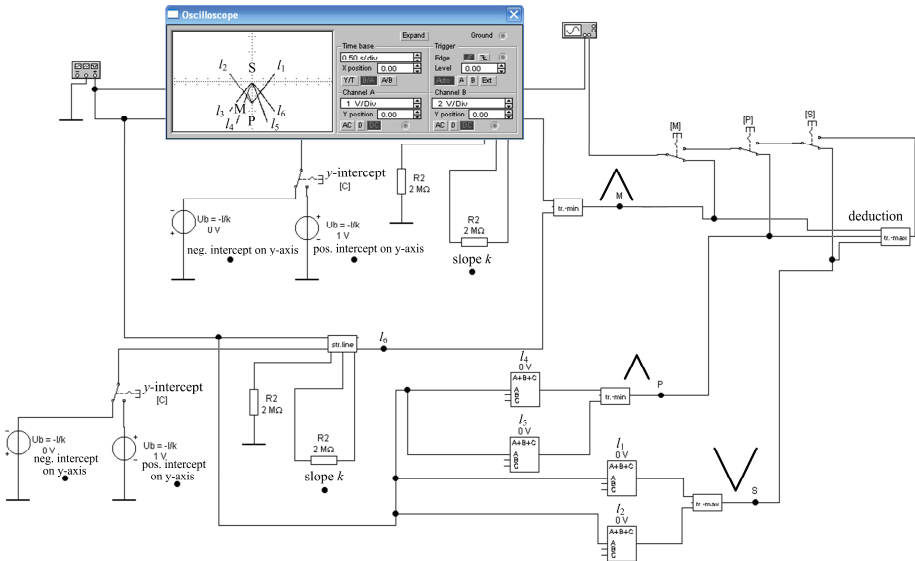|	
Baroco	
All P are M	*All informative things are useful.*
Some S are not M	*Some websites are not useful.*
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Some S are not P	*Some websites are not informative.*

Fig. 9. Hardware model of figure *Baroco*

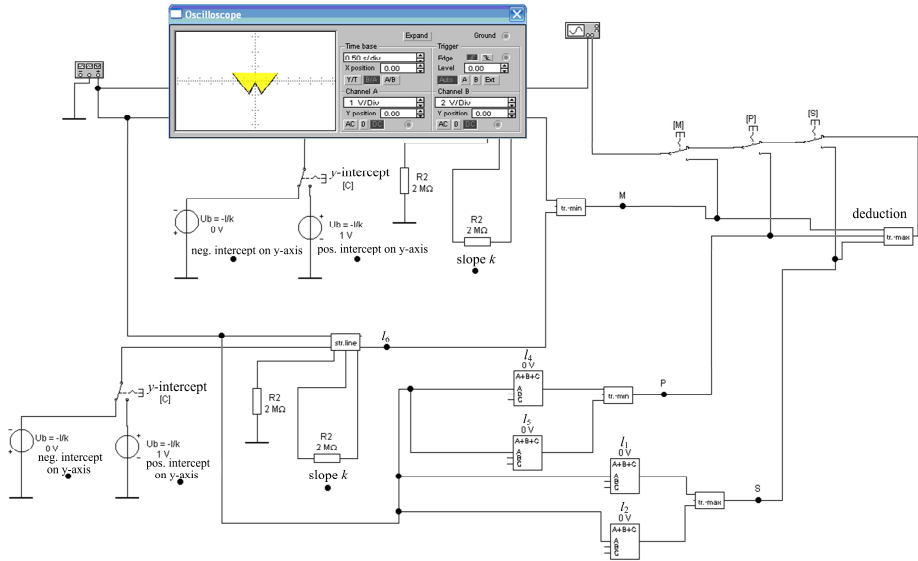Graphic representation (an oscillogram) of relations between terms in figure *Baroco* is shown in Fig. 10.

Fig. 10. "Hardware deduction" for figure *Baroco*: max $(S, P, M) \equiv$ some S are not P

Function generator plays the role of a universe of discourse and can be related with an output limiter (not shown in the model) which limits output voltage to an arbitrary output expressed as $\min(U_A, \max(U_S, U_P, U_M))$ where voltages U_S, U_P, U_M represents sets S, P and M respectively, and U_A is an arbitrary limiting voltage.

Valid mood of categorical syllogism called *Darii*

Darii	
All M are P	All cypress trees are evergreens.
Some S are M	Some trees are cypress trees.
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Some S are P	Some trees are evergreens.

can also be modeled in the analog hardware circuit environment (see Fig. 11 and 12). Note that a different hardware approach, based on semicircle generators and square root circuits along with dedicated *min-max circuits*, is used in this *Darii*-hardware model [9].

Test circuits showed before (see Fig. 5, 6 and 7) can be used to check the validity of "hardware deduction", i.e. conclusion in both models. The simplest way to interpret "hardware deduction" is to use simple passive integrator as shown in Fig. 13.

Hardware circuit models of other figures can be a part of *future work*, together with the interpretation of their effect in a *hardware model of system control*.
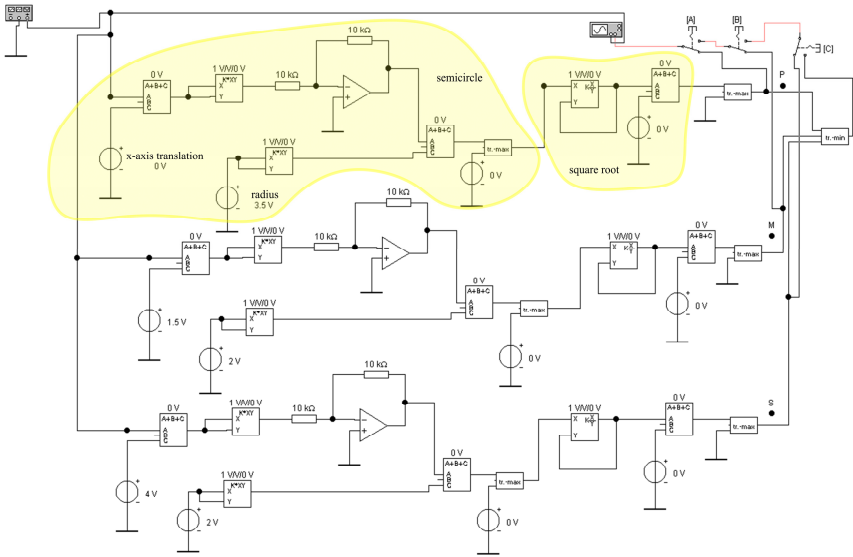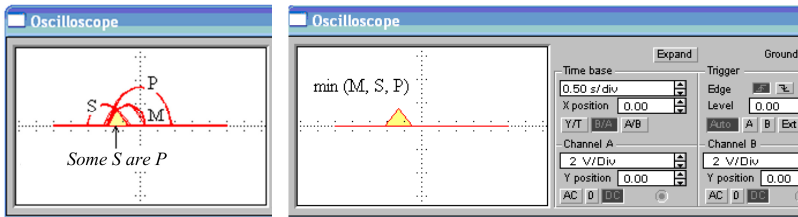
Fig. 11. Hardware model of figure Darii: Some S are P

Fig. 12. "Hardware deduction" (conclusion) for figure Darii: some S are $P \equiv$ min (M, S, P) where M, S and P stand for related voltages U_S, U_P and U_M
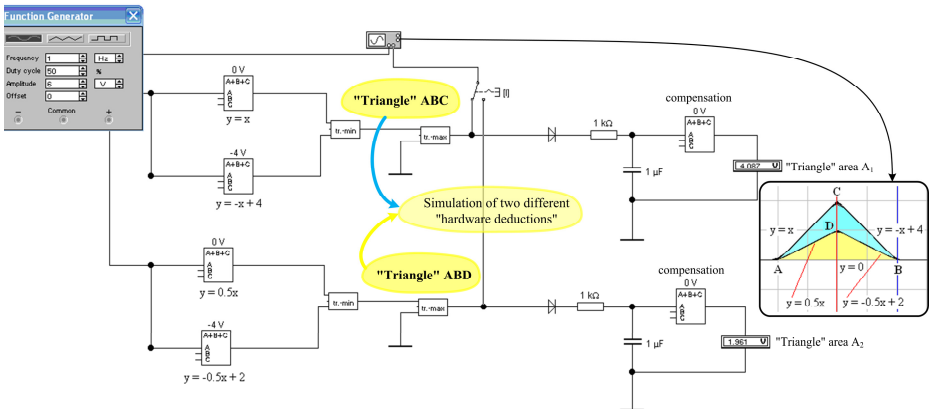

Fig. 13. Simple interpretation of "hardware deduction" There are more S_1s in P_1s then S_2s in P_2s, therefore $A_1 : A_2 = 2 : 1$

4   Conclusion

In this paper, we have shown that is possible to model syllogism(s) and to interpret deduction process as an voltage in analog hardware environment by using original operational amplifier based platform. The platform consists of original min-max circuits and straight-line generators.

The basic advantage of this method in modeling thinking rational approach can be summarized as follows: simple circuitry, no special hardware design (devices) is (are) necessary, simple definition terms are easy to obtain, comprehensible, inexpensive, student (education) oriented and many useful laboratory experiments at an undergraduate level can be performed.

Hardware models of syllogisms can be used as response modulators of the adaptive process control machine that is based on a learning transfer characteristic [10].

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