Optimization-Based Design of Nano-CMOS LC-VCOs

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Abstract. This paper introduces a variability-aware methodology for the design of LC-VCOs in Nano-CMOS technologies. The complexity of the design as well as the necessity for having an environment offering the possibility for exploring design trade-offs has led to the development of design methodologies based multi-objective optimization procedures yielding the generation of Pareto-optimal surfaces. The efficiency of the process is granted by using analytical models for both passive and active devices. Although physics-based analytical expressions have been proposed for the evaluation of the lumped elements, the variability of the process parameters is usually ignored due to the difficulty to formalize it into an optimization performance index. The usually adopted methodology of considering only optimum solutions for the Pareto surface, may lead to pruning quasi-optimal solutions that may prove to be better, should their sensitivity to process parameter variation be accounted for. In this work we propose starting by generating an extended Pareto surface where both optimum and quasi-optimum solutions are considered. Finally information on the sensitivity to process parameter variations, is used for electing the best design solution.

Keywords: VCO optimization, CMOS parameter variability, sensitivity analysis, integrated inductor.

1 Introduction

The rapid evolution of the CMOS technology has made possible the development of smaller communication systems with increasing functionality. Yet, as CMOS technology approaches the nano-scale, significant deviations in the system performance may be found due to either interconnect or device inter- and intra-die parameter variations. Generally, in nano-CMOS technology, imperfections in analog and digital circuits are commonly referred as process's parameter variability. Parameter variability is a consequence of several physical processes, which occur during fabrication, such as line edge roughness, random dopant fluctuations and oxide thickness variations [1]-[3]. Since process variability has strong influence on circuit reliability as well as in the circuit lifetime, designers usually are tempted to use large design margins, degrading the circuit performance. In order to overcome these issues, reliable assess-

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ments must be done at design time [1]. The need for obtaining variation tolerant physical designs forces the adoption of new design methodologies, where both parasitics and process variability are accounted for. In addition to new design methodologies, as circuit specifications are becoming more stringent mainly for wireless devices, efficient device models are needed in order to reduce mismatches between expected and real circuit performance [4].

In his paper the design of LC-VCOs is addressed. Due to the high-density integration needs as well as to low cost fabrication, RF applications are usually implemented in CMOS technology. However, this technology development brought up several issues such as the degradation of on-chip inductor's quality factor, due to thin metal thickness and substrate losses yielding VCO's phase noise limitation owing to the tank low quality factor [5]. Yet, as the process technology improves and the number of metal layers increases, the Q of the passive elements is improving [6].

In Fig. 1 a schematic representation of an LC-VCO design architecture is presented.

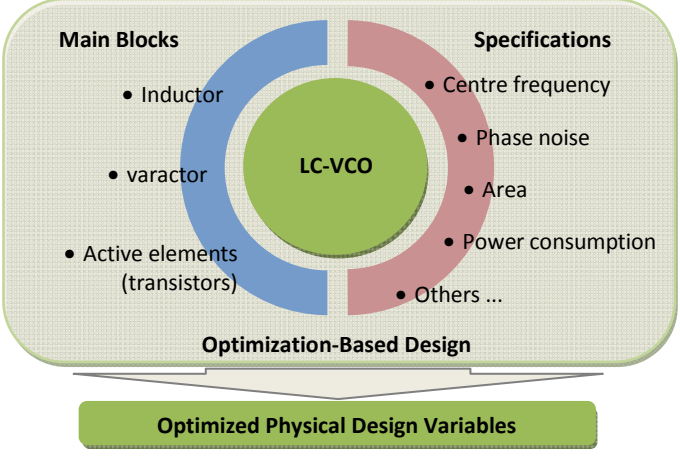


Fig. 1. LC-VCO design architecture

As the design of an LC-VCO may involve many metrics that conflict to each other, with respect to design parameters, optimization–based methodologies are usually adopted. For the efficiency of the design process, analytical models for both passive and active devices must be considered. As far as the active devices are concerned, accurate process dependent transistor models including parasitics effects can be found in the literature. As for the minimization of the active devices variations, several techniques such as silicon strain and high-K gate dielectric, among others, have been proposed as a way of maintaining transistors performance in spite of the ever-diminishing device sizes [7], the variability of the active devices parameters will not be considered in this paper. Yet the need for using integrated inductors raises additional modelling needs where the variability of the metal width, the spacing between conductor and the thickness of interlayer dielectrics must be taken into account. In

general, although a SPICE simulation tool can perform accurate circuit analysis, it is not capable to evaluate the robustness of device regarding design variables.

Designers have been dealing with such analytical relations mostly by experience, rather than by using simulation tools [8]. The circuit robustness against process parameter variability may be characterised through the circuit *sensitivity* to design parameter. The benefit of sensitivity analysis is to offer the availability of an analytical function for one or more circuit parameters as well as the possibility to understand which parameter/device has a stronger or weaker influence on the circuit performance [8] and [9].

In this paper, we propose using an optimization-based design methodology applied to nano-CMOS LC-VCO. The remaining of the paper is organized as follows. The novelty introduced by this paper, as well as the LC-VCO optimization strategy, is offered in Section 2. The inductor characterization, which includes the inductor model and sensitivity analysis, is presented in Section 3. Then, Section 4 is dedicated to the optimization examples, where the focus is on the inductor sensitivity analysis. Finally, conclusions are offered in Section 5.

2 Contribution to Value Creation

The main objective of the LC-VCO optimization-based design methodology presented in this work is to generate the geometrical layout parameters of the full circuit, meeting the design specifications. Yet, to achieve this goal, several issues, such as the process variability and accurate analytical models must be taken into consideration in order to guarantee the accuracy and robustness of the results.

The novel contributions of this paper are as follows:

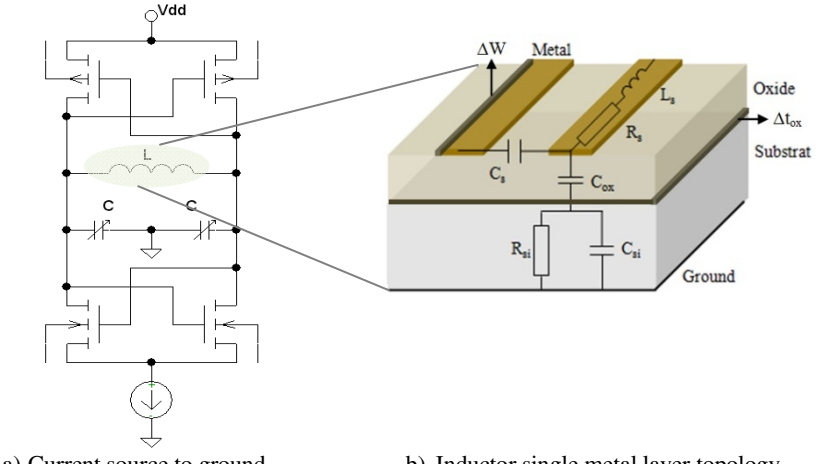
- This paper proposes an optimization-based design for nano-CMOS LC-VCO, obtaining solutions in an efficient way based in analytical models, instead of using a simulation based approach;
- The different stages of the design flow, which will be undertaken in deep analysis in future research, are identified;
- The use of evolutionary algorithms, as a step to obtain the best design solution, based on the information of sensitivity to process parameter variations, is addressed.

2.1 LC-VCO Design

When designers have in hands the task of designing a VCO, one of the main challenges is to obtain results between simulation and on-chip measurement as close as possible. For this propose, accurate models are essential for each of the circuit blocks, where parasitics, as well as process variability, must be accounted for. In Fig. 2 a typical LC-VCO topology is presented, where the inductor structure is highlighted, as an example of circuit parasitics and process variability (ΔW, Δt_{ox}).

As can be seen in the Fig. 2, a VCO has two main blocks; the LC thank responsible for the oscillation frequency, and the active circuit which is responsible for reducing the circuit losses by introducing a negative resistance. Most of the LC-VCO designs have as main criteria to achieve both minimum phase noise and minimum power

consumption for a certain oscillation frequency. In a very simplistic point of view, for a specified frequency, the design problem to be worked out is the dimensioning of all the elements of the LC-VCO. As the relationship between the design variables is very complex, several design methodologies have been proposed in the literature.



a) Current source to ground b) Inductor single metal layer topology

Fig. 2. LC-VCO topology

For the dimensioning of the LC-VCO, the design methodologies that are usually adopted have its essential pillar on the models of each element. Even though designers may use very accurate models, for predicting the VCO performance, there will always be a certain error due to some parasitic effects that appear in the manufacturing process [10]. For that reason a VCO is always tunable. In the recent years, with the advent of CMOS technologies approaching the nano-scale, besides the parasitic effects, the process variability due to fabrication and/or lifetime degradation must also be considered, leading to the study of the circuits´ sensitivity [11]-[14].

Regarding the optimization procedure, a complete description of an integrated LC-VCO design is presented in [15], where the complexity of the optimization design, regarding the number of variables involved, is focused. A graphical optimization methodology which uses graphical nonlinear programming is proposed, providing essential intuitions in finding the optimum solution. Another optimization methodology, where electromagnetic simulators as Cadence SpectreRF and ASITIC are used as a way to guarantee the accuracy of results, is presented in [16]. Here, the LC-VCO design optimization is based on the gm/ID methodology, where the oscillator design space is studied with the goal of obtaining the optimum design, considering phase noise – consumption trade-off. In [17] a graphical optimization method is presented. In this work, design constraints are graphically represented in order to give the designer an overview of the correlation between the design parameters. The results obtained by analytic form are verified with simulation using ADS software. All the three optimization methodologies presented above, suffer from the lack of circuit sensitivity analysis.

In this paper a variability aware LC-VCO design methodology is proposed. The optimization-based design flow for the proposed methodology is represented in Fig. 3. Having in mind the LC-VCO topology illustrated in Fig. 2, for a given set of specifications, the design process starts with the design of the active elements, since the drain current in each transistor is the dominant contributor to the phase noise. The following step aims to optimize the LC tank design, improving the quality factor. The LC tank is the main block on a LC-VCO. Therefore, the optimization procedure will test the circuit robustness, regarding the design variables/process variability, for *n* different design combinations that meet design specifications, by analysing the circuit sensitivity. In the end, if all requirements are met, the final designs are integrated into the Pareto Front.

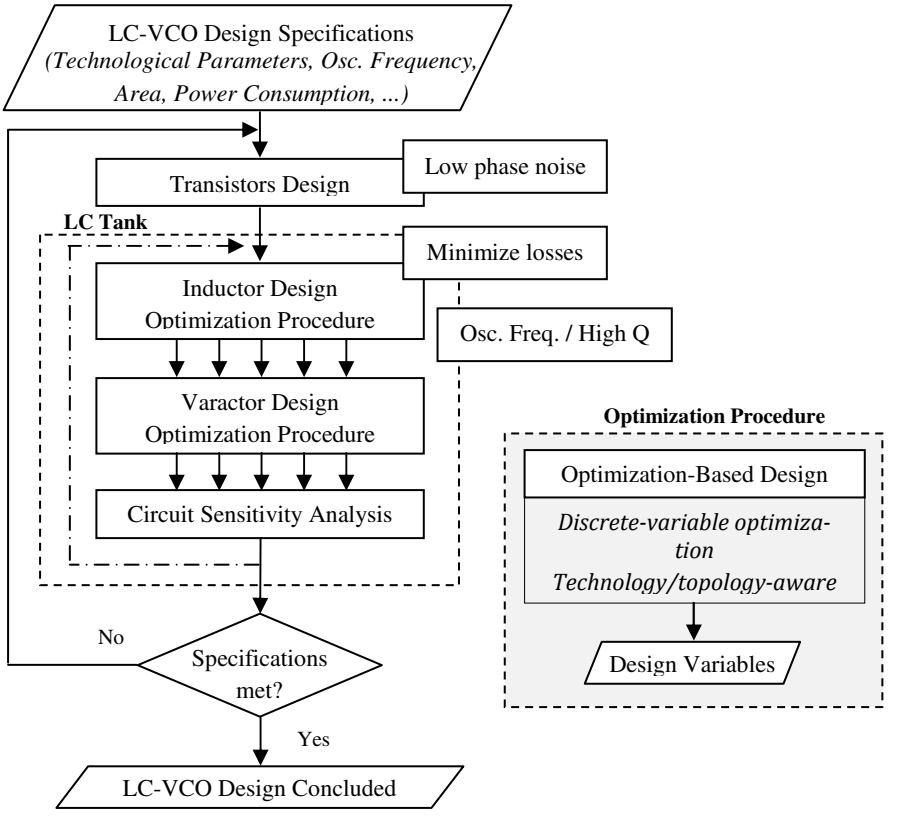


Fig. 3. Optimization-Based Design flowchart

The following sections are dedicated to the optimization of the inductor, since it is the most critical element on a LC-VCO.

3 Inductor Characterization

Generally, for the efficiency of the optimization process, analytical models are used for the passive/active devices. With respect to the inductor, and for the sake of simplicity the pi-model, illustrated in Fig. 4, is adopted. Albeit, the authors have been working in a more complex inductor model [18], for the clarity of exposure concerning circuit sensitivity analysis, the inductor pi-model enables a better acquaintance on the subject.

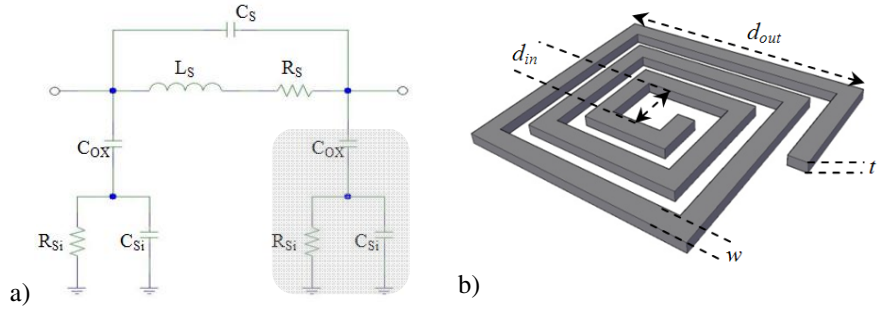


Fig. 4. Integrated spiral inductor: a) Planar inductor pi-model, b) Layout of a square inductor

The inductor quality factor (Q) is usually adopted as the characteristic to be used when comparing inductors performance. For an accurate prediction of Q, the parasitic effects cannot be neglect. The pi-model presented in Fig. 4 takes into account a set of various parasitic and loss elements, allowing to write (Q) as a function of the passive components. The Q is usually calculated reducing the two ports of the pi-model, to a single port by grounding the second port (shadow branch) [19]. This configuration aims to simplify the analysis of the Q behaviour. The Q is analytically obtained by

$$Q = \frac{\omega L_S}{R_S} \frac{R_P}{R_P + \left[\left(\frac{\omega L_S}{R_S}\right)^2 + 1\right] R_S} \left[1 - \frac{R_S^2}{L_S}(C_S + C_P) - \omega^2 L_S (C_S + C_P)\right], \tag{1}$$

where

$$R_P = \frac{1}{\omega^2 C_{ox}^2 R_{si}} + \frac{R_{si}(C_{ox} + C_{si})^2}{C_{ox}^2} \tag{2}$$

$$C_P = C_{ox} \frac{1 + \omega^2 (C_{ox} + C_{si}) C_{si} R_{si}^2}{1 + \omega^2 (C_{ox} + C_{si})^2 R_{si}^2}. \tag{3}$$

3.1 Sensitivity Analysis

For the pi-model adopted the physics-based analytical expressions have been proposed for the evaluation of the lumped elements. Yet, the variability of the process

parameters is usually ignored due to the difficulty to formalize it into an optimization performance index. The *sensitivity* of a circuit is the capacity to react with changes in certain parameters. It is considered as a measure of how the circuit responds to an undesirable parameters variation.

Let $H(s)$ be a transfer function of a ordinary circuit. The sensitivity is defined to be the relative variation of $H(s)$ with respect to the variation of a circuit parameter, p, defined by

$$Sen_p^{H(s)} = \frac{p}{H(s)} \frac{\partial H(s)}{\partial p}. \tag{4}$$

Several works have been published in the recent years, regarding sensitivity analysis. As the number of elements in a circuit grows, analytical analysis becomes unfeasible either due to the complex relation between parameters or to the device models. In this case, the strategy adopted in recent publications is a symbolic calculation method based on binary decision diagram or graph-pair decision diagram [20]-[22].

As mentioned before, the inductor pi-model, due to its simplicity, allows an analytical characterization regarding circuit sensitivity. In Fig. 5 the relationship between three fabrication level parameters and the inductor Q and inductance, L, is illustrated. For details concerning the pi-model equations, please see [23].

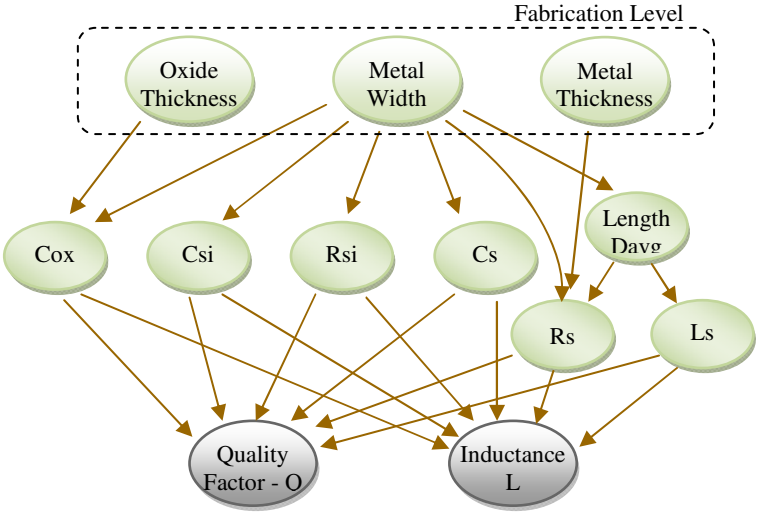


Fig. 5. Process variables impact on inductor quality factor and inductance

According to [20], for a set of design parameters depending on a process variable, the circuit sensitivity can be computed by the following equation

$$Sen_{p_k}^{H(s)} = \sum_{i=1}^{m} Sen_{a_k^i}^{H(s)} . Sen_{p_k}^{a_k^i}. \tag{1}$$

In Fig. 5 the inductor Q is dependent on C_{ox}, which is dependent on oxide Thickness, t_{ox}. Taking into account equation (4), the quality factor sensitivity with respect to oxide thickness, is given by

$$Sen_{t_{ox}}^{Q} = Sen_{C_{ox}}^{Q} \cdot Sen_{t_{ox}}^{C_{ox}}. \tag{2}$$

Moreover, the quality factor sensitivity concerning both oxide thickness and metal thickness, according to (5) can be obtained by

$$Sen_{t_{ox},M_t}^{Q} = Sen_{t_{ox}}^{Q} + Sen_{M_t}^{Q} = Sen_{C_{ox}}^{Q} \cdot Sen_{t_{ox}}^{C_{ox}} + Sen_{R_S}^{Q} \cdot Sen_{t_{ox}}^{R_S} \tag{3}$$

4 Optimization of Inductor Design

The complexity of the design as well as the necessity for having an environment offering the possibility for exploring design trade-offs has led to the development of design methodologies based multi-objective optimization procedures yielding the generation of Pareto-optimal surfaces. This section is dedicated to the optimization of an integrated spiral inductor. The methodology adopted aims to achieve a technology/topology-aware solution, where the inductor sensitivity to the oxide thickness is explored as a way to guarantee circuit robustness. Also to be accounted for is the discrete nature of the design variables, as well as, the correlation between them. The optimization tool is implemented in Matlab and uses the optimization toolbox.

The design concerns the evaluation of four independent parameters, namely the track width (w), the number of turns (n), inductor shape (N_{side}), and the internal diameter (d_{in}). In this section the design of a 5 nH inductor for an operating frequency of 0.7 or 1.0 GHz for UMC130 technology is addressed, where the technological and physical parameters are shown in Table 1. The determination of the layout parameters is done according the optimization methodology in [19], where a maximum tolerance in the inductance value, δ, of 5%, is imposed. The inductor design may be seen as a multi-objective problem; however, for the simplicity of the optimization algorithm, some of the objective functions were included as a series of constraints.

In this example the inductor layout parameters yielding the maximum quality factor are generated. A maximum output diameter of 600μm is considered, as well as the tolerance, δ, of 5% is guaranteed. The optimization problem can be symbolically represented by

$$\begin{aligned} &Maximize \quad Q(n, d_{in}, w, s) \\ Subject\ to \quad &(1-\delta) \cdot L_{expect} \le L(n, d_{in}, w, s) \le (1+\delta) \cdot L_{expect} \end{aligned} \tag{8}$$

The optimization tool generates a set of points, which belong to a Pareto front, that will be evaluated regarding its sensitivity to oxide and metal thickness, t_{ox} and t respectively.

Table 1. Physical Parameters of Inductor Design

Parameter	Value	Parameter	Value
Metal Thickness	2.8 μm	Oxide Permittivity (ε_r)	4
Space betwwen turns	2.5 μm	Susbtrate Thickness	700 μm
Sheet Resistance	10 mΩ/square	Susbtrate Permittivity (ε_r)	11.9
Oxide Thickness	5.42 μm	Susbtrate Resistivity	28 Ω.cm
Oxide Thickness between spiral and underpass	0.26 μm		

Table 2. Spiral Inductor Design Constraints

Parameter	Min	Step	Max
w (μm)	5.0	0.5	100.0
d_{in} (μm)	20.0	0.5	200.0
n	1.5	1.0	15.5
N_{side}	Square (4) / Hexagonal (6) / Octagonal (8)		

The optimizations results for the design of a 5 nH inductor, for operating frequencies of 0.7 and 1.0 GHz are shown in Tables 3 and 4, in that order.

Regarding the results in Table 3 and 4, it is also possible to conclude that there is a commitment between Q and d_{out} ,i.e., when maximizing Q, the largest area is chosen. All the solutions present the same number of turns and geometric configuration. Regarding to the circuit sensitivity analysis, Sens(Q(t_{ox},t)), the sensitivity drops as the quality factor increases. This fact is explained by the fact that as large the metal track width becomes, the metal resistance stays less dependent on metal thickness. On the other hand, as can be seen in Table 5, the Q can be considered t_{ox} independent. As stated, the solution with the highest Q, is also the one that presents the lowest sensitivity. A sensitivity of 0.73, means that a change of 1% in the inductor parameters, corresponds to a variation of 0.73% in the quality factor.

In Table 5, the sensitivity of the quality factor to the variability of each of the parameters analysed, is presented. Here it is possible to confirm that the quality factor presents almost total immunity to t_{ox} variability. The Q sensilibility to t_{ox} is 0.012, in the case of a 5 nH inductor (0.7 GHz), which can be ignored. Although, and for the same inductor, the Q sensitivity regarding the metal thickness is 0.714.

With the sensitivity facility offered by the proposed tool, besides the optimization design procedure, it is possible to have extra information that would help designers to have a proper decision regarding circuit robustness to process variability.

Table 3. Optimization results for an inductor of 5 nH, 0.7 GHz

w (µm)	d_{in}(µm)	N_{turns}	N_{side}	d_{out}(µm)	L(nH)	Q	Sens(Q(t_{ox},t))
20.0	126.0	4.5	8	324	5.12	11.26	0.82
23.0	122.5	4.5	8	347	5.11	12.03	0.80
23.5	122.0	4.5	8	351	5.11	12.15	0.79
24.0	121.5	4.5	8	355	5.12	12.27	0.79
39.5	**199.0**	**3.5**	**8**	**488**	**5.02**	**15.44**	**0.73**

Table 4. Optimization results for an inductor of 5 nH, 1.0 GHz

w (µm)	d_{in}(µm)	N_{turns}	N_{side}	d_{out}(µm)	L(nH)	Q	Sens(Q(t_{ox},t))
20.0	123.0	4.5	8	321	5.11	14.55	0.74
23.5	117.5	4.5	8	347	5.09	15.37	0.72
33.5	190.5	3.5	8	438	4.88	17.69	0.66
37.0	187.0	3.5	8	459	4.9	17.92	0.64
37.5	**188.5**	**3.5**	**8**	**464**	**4.95**	**17.92**	**0.63**

Table 5. Sensitivity to Variations in Oxide (t_{ox}) and Metal Thickness (t)

Process variation		5 nH, 0.7 GHz				5 nH, 1.0 GHz			
Oxide thickness	Metal thickness	Sens Q(t_{ox})	Sens Q(M_t)	Q_{min}	Q_{max}	Sens Q(t_{ox})	Sens Q(M_t)	Q_{min}	Q_{max}
± 10 %	0 %			15.42	15.46			17.89	17.94
0 %	± 10 %	0.012	0.714	14.33	16.51	0.013	0.617	16.82	19.00
± 10 %	± 10 %			14.28	16.52			16.75	19.00

5 Conclusions

This paper introduces the circuit sensibility analysis integrated in an optimization-based design of nano-CMOS LC-VCOs. For the sake of simplicity, the simple pi-model was considered in the present work. The model is supported by a set of equations based exclusively in technology parameters instead of equations obtained by fitting process of measure data. As models do not take into account process variability, sensibility analysis offers the availability of an analytical function for one or more circuit parameters, providing extra knowledge about circuit robustness concerning to process variability.

In this work the design of RF integrated inductors is supported by a optimization methodology, where constraints on the values of the variables representing the layout parameters are used. This enables the generation of the best solution for the technology used.

The working examples showing the design of an inductor for 5 nH, and operating frequency of 0.7 and 1.0 GHz are presented, where the sensitivity analysis is highlighted.

The main limitation of the work proposed resides in the simple pi-model used, as it is not applicable for frequencies higher than 1GHz. However, it enables the possibility of having analytical function for the sensitivity characterization. Typically, when using more complex models, the sensitivity analysis is computed by mathematical algorithms, such as Monte Carlo.

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