"Single-chip Cloud Computer", an IA Tera-scale Research Processor

Jim Held

Intel Fellow & Director Tera-scale Computing Research
Intel Labs, USA
jim.p.held@intel.com

Abstract

As part of our Tera-scale Computing Research Program, Intel Labs has created a second generation experimental "Single-chip Cloud Computer" (SCC). It contains the most Intel Architecture cores ever integrated on a silicon CPU chip: 48 cores. It incorporates technologies intended to scale multi-core processors to 100 cores and beyond, such as an on-chip network, advanced power management technologies and support for *message-passing*.

Architecturally, SCC is a microcosm of a cloud data-center. Each core can run a separate OS and software stack and act like an individual compute node that communicates with other compute nodes over the on-die packet-based network fabric, thus supporting the "scale-out" message passing programming models that have been proven to scale to 1000s of processors in cloud data-centers.

The SCC serves as an experimental platform for a wide range of software research and is currently being used by a worldwide community of academic and industry co-travelers. This talk will describe the architecture of the SCC platform and discuss its role in the broader context of our Tera-scale research. For more information, see www.intel.com/info/scc

Short Biography

Jim Held is an Intel Fellow who leads a virtual team of architects conducting Tera-Scale Computing Research in Intel Labs. Since joining Intel in 1990, he has led research and development in a variety of Intel's labs concerned with media and interconnect technology, systems software, multi-core processor architecture and virtualization. He earned a Ph.D. (1988) in Computer and Information Science at the University of Minnesota.

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