

Automated Design Approach for Analog Circuit Using Genetic Algorithm

Xuewen Xia¹, Yuanxiang Li², Weiqin Ying², and Lei Chen¹

¹ School of Computer Science, Wuhan University, Wuhan 430079, China

² State Key Lab. of Software Engineering, Wuhan University, Wuhan 430072, China
laughkid@163.com

Abstract. The technology of electronic design automation (EDA) has improved the efficiency of design process, however, designer is still required much special knowledge of circuit. During the past decade, using genetic algorithm (GA) to design circuit had attracted many experts and scholars. However, too much more attention was focus on a circuit's function and many other factors had been neglected which caused the circuit had little applicability. This paper proposes an automated design approach for analog circuit based on a multi-objective adaptive GA. The multi-objective fitness evaluation method, which can dynamic adjust parameter, is selected. And a parallel evolution strategy which separates evolution of circuit structure and element value is adopted but also organically combined them by weight vectors. The experimental results indicate that this approach obviously be able to improve the evolution efficiency and could generate numbers of suitable circuits.

Keywords: Evolutionary algorithms, Electronic Design Automation, Evolving hardware.

1 Introduction

In contrast to conventional circuit design where the designers were required much special knowledge of circuit, Evolvable Hardware (EHW) technology needs fewer designers' intervention and special knowledge of circuit during the design process.

Evolutionary Hardware uses techniques derived from evolutionary computation such as genetic algorithm and genetic programming to develop electronic circuits, which capable of solving real world problems. The researches of Koza [1] and his collaborators on analog circuit synthesis through genetic programming [2] (GP) is likely the most successful evolutionary computation-based approach so far, but this approach, like many other experiments, indicated that design an applicable circuit, especially analog circuit, is very time-consuming [3], and even is infeasible. Therefore, various experiments on speeding up the GA computation have been undertaken [4], and other approaches to the problem have been undertaken by using variable length chromosome [5].

In this paper, a simple encoding scheme based on Spice Netlist file format is selected. And a dynamic adjusting method based on evolutionary strategy which could improve the evolution efficiency is selected. Two representative analog

circuits are adopted to test the approach because design analog circuit is more difficult than design digital circuit.

The paper is organized as follows. The approach of evolving analog circuits, includes the presentation of circuit, the evolutionary strategy and the evaluation method are introduced in section 2. In section 3, the results of experiment and analysis are presented. At last, a conclusion is provided.

2 Approach of Evolving Analog Circuits

2.1 Encoding and Decoding Scheme

It is an elementary problem in evolvable hardware that to chose a suitable method of encoding and decoding. In general, there are two methods: Global encoding, which refers to encoding with all information of a circuit, and local encoding, which refers to encoding with the part information of a circuit. The latter method is selected in this paper in which the circuit has been separated into two parts: structure part and element value part. And these two parts are respectively evolved with each local coding.

Instead of some detailed requirements to initialize the circuit, there are only the numbers of elements and the type of it should be defined advance according to the experiential knowledge of circuit's complexity.

For the structural evolution, the type and link-nodes of elements are encoded into binary code, but the value of it is not included. The number of an element's nodes is determined by the maximum nodes that the element has.

$$E_1 = [Type, Node_1, Node_2, \dots, Node_n]. \quad (1)$$

In (1), *Type* denotes the index of element type, while *Node_i* ($i \in [1, n]$) denotes each link-node of element. The value of element is random generated at the beginning of evolution process. The chromosome of a circuit is composed of every element's binary code which linking with each other.

For the value evolution, the code is almost the same as structure evolution, but the element's value is, instead of link-node, encoded.

$$E_2 = [Type, Value_1, Value_2, \dots, Value_m]. \quad (2)$$

In (2), the *Value_i* ($i \in [1, m]$) denotes many different parameters of an element, and the number of the element's value is determined by it's *Type*. For example, the resistivity and the linear temperature-coefficient are selected to be parameters of a resistance.

Before simulated by SPICE emulator, these two results (structure and elements) should be combined in order to get the whole information of a circuit. Firstly, the set of element from structural evolution should be decoded individually, so the type of each element could be acquired by table querying, and every link-nodes of element should be recorded in order to obtain the topology of circuit. Then the set of value of each element should be obtained by decoding the

set of element from value evolution. Finally the whole data of each element in the circuit are presented. The format could be described as follow:

$$E = [Type, Node_i, Value_j]. \quad (3)$$

2.2 Simulate Circuit with Pretreatment Code

wing to the features of genetic algorithm's encoding model and the operators of it, the element's link condition might not be directed properly. It may cause some topology errors which could result in more than fifty percents of circuits be illegal, which would obviously decrease the efficiency and feasibility of evolution because majority of time is spent on the simulating during the process. To avoid this case, the circuit must be pretreated and be checked for these cases:

1. Less than 2 connections at a node;
2. No DC path to ground from a node;
3. Inductor/voltage source loop found.

These errors could be obtained by scanning the circuit advance, and then corrected or deleted them, as a result, the circuit's validity could be guarantied to some extend.

At last, combining the whole valid circuit's information and the commands of output data, a regular SPICE Netlist file would be generated, hence the simulation could be proceed successfully by software SPICE.

2.3 Evolutionary Strategies Based on the Dynamic Adjusting Weight Vector

Since rates of mutation and crossover influence the efficiency of genetic algorithm, so they should be altered along with evolution process and the fluctuation of environment. Because of the parallel two layers evolutionary strategy, mutation rates (P_{sm}) and crossover rates (P_{sc}) of structural evolution have relations to those of value evolution. With the increasing generation and the rates of fitness, P_{sm} and P_{sc} of structure and value will became less.

$$P_{sm} = K_1(1 - \exp(-\frac{dFitness}{dGeneration})) \quad (4)$$

$$P_{sc} = K_2P_{sm} \quad (5)$$

In the equations above, $K_1 \in (0, 1), K_2 \in (0, 1)$.

$$P_v = \exp(-(P_{sc} + P_{sm})) \quad (6)$$

After the start of value evolution, the rates of mutation and crossover resume in order to preventing local convergence. Based on the traditional theory of evolutionary algorithm, the algorithm could not search effectively after the population had con-verged [6,7]. The approach in this paper could obtain optimal parameters from sorts of circuit, so it overcome local convergence during the early period, and also avoid some cases that one circuit been eliminated for its unsuitable element value.

2.4 Fitness Evaluation Method

The quality of evaluation function influences the result and the process of analog circuit's evolution greatly. A precisely comprehensive evaluation strategy would direct evolution to a more efficient process, which could obtain a more suitable result in a relative short period.

In this paper, an offline evolution model based on SPICE software has been selected, and a multi-objective fitness evaluation function is adopted in order to meet many design objectives. The fitness of circuit is described as:

$$Fitness = f(g, s, p) \quad (7)$$

The vector g denotes the optimization degree of a circuit performance, s denotes the number of type of elements, and p denotes the scale of a circuit. The experiences of design during past remind us that a good circuit should have less kinds of elements and small scale besides good performance. In this paper, function f is described as follow:

$$f(g, s, p) = c_1g + c_2s + c_3p, \quad \sum_{i=1}^3 c_i = 1 \quad (8)$$

In (8), c_i is weight vector which could be used to adjust the weight of three parameters according to designer's demands.

The performance of a circuit is determined by many aspects, so the vector g should be defined to be diversified function according to different design objectives. Owing to the separated parallel evolution mode, the fitness of circuit's structure and element value could be separated into two different functions. In the experiment of transistor amplifier design, a stable amplifier is the destination of structural evolution, while its amplification ratio is the mission of value evolution. When a low-pass filter is designed, the structural evolution will take charge of low-pass performance, and the feature of frequency and voltage are left to value evolution to be obtained. The evaluation strategy of transistor amplifier's structure is to analyze the curve from transient analysis.

The evaluation function is $g_1(x)$ that expressed by (9). The vector α is a weight vector, $V_o(x)$ and $V_i(x)$ respectively denotes the voltages of output and input. Function $h_1(x)$ evaluates the stability of amplification of output voltage, and function $e(x)$ evaluates the AC work state of Bipolar Junction Transistor from individual x in order to guarantee a stable working condition to the transistor in its value domain. The value evaluation function is $g_2(x)$ that expressed by (10). The vector A is an expectant voltage gain, and function $h_2(x)$ will evaluate the difference between the expectant outcome and the experimenter's.

$$g_1(x) = \alpha h_1 \sum_m \left(\frac{v_{om}(x)}{v_{im}(x)} - \frac{v_{om-1}(x)}{v_{im-1}(x)} \right)^2 + (1 - \alpha)e(x), \quad \alpha \in (0, 1) \quad (9)$$

$$g_2(x) = \alpha h_2 \sum_m \left(A - \frac{v_{om}(x)}{v_{im}(x)} \right)^2 + (1 - \alpha)e(x), \quad \alpha \in (0, 1) \quad (10)$$

The evaluation strategy of a low-pass filter structural evolution is to analyze the curve from frequency analysis. The fitness function is $g_3(x)$ that expressed by equation (11). $v_{max}(x)$ and $v_{min}(x)$ respectively expresses the maximum and minimum of output curve, $p(x)$ and $q(x)$ are pass-cutoff point and reject-cutoff point that could be measured by extremum analysis method. Extremum analysis method is based on comparing every extremum point with $v_{max}(x)$ to insure the position of pass-cutoff point and reject-cutoff point, and analyzing the region between the two points combine with each point's slop or differential coefficient to insure pass-cutoff frequency f_p and reject-cutoff frequency f_r .

$$g_3(x) = \beta h_3 \left(\sum_{i=1}^{p(x)} (v_{max}(x) - v_{oi}(x)) + \sum_{i=q(x)}^n (v_{oi}(x) - v_{min}(x)) \right), \beta \in (0, 1) \quad (11)$$

The evaluation strategy of low-pass filter value evolution is almost the same as that of the transistor amplifier. Evaluating the difference between experimental and expectant value of voltage gain and feature frequency, combining with evaluating work state of operational amplifier, the outcome of value evolution could be obtained.

3 Experimental Results and Analysis

In this paper, two kinds of circuits, passive filter and amplifier, are experimented because that with the following reasons:

1. Filter circuit includes resistance, capacitor, and inductance, therefore the circuit's configuration is very simple and it is easy to analyze the circuit. Furthermore, the analysis of input-output characteristics of passive filter is representative which involves many parameters of analog circuit.
2. Most analog circuit could be made up of resistance, capacitor, inductance, and dynatron. So an amplifier circuit which includes dynatron could represent majority structure of analog circuit.
3. When making an appraisal for a passive filter and amplifier, many design objectives should be considered, so the search of these circuits could testify the validity of multi-objective evaluation strategy proposed by this paper.

The parameters of evolution are set as follow that maximal number of element is 20, maximal number of node is 8, max generation is 2000, size of population is 60 (40 for structure and 20 for value), initial rate of mutation and crossover was $P_m=0.1$, $P_c=0.03$.

3.1 Experiment 1

In this experiment, the objectives of transistor amplifier are prearranged that voltage magnification is 350, the generate ratio of resistor, capacitance, power supply, and transistor is 6:3:1:2.

A relative good circuit has been obtained after 800 1000 generations, and a perfect circuit has selected to demonstrate in Figure.1:

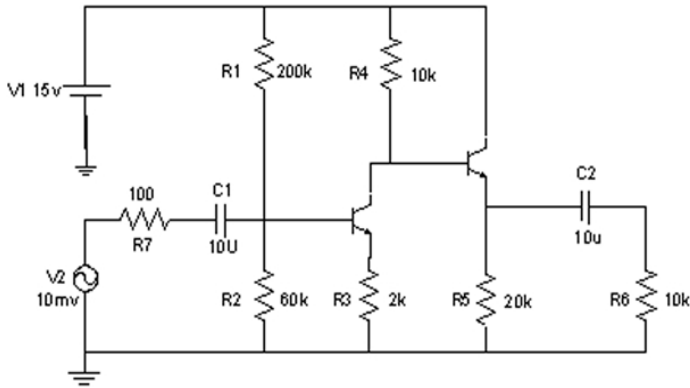


Fig. 1. The best voltage amplifier structure from generation 1000

3.2 Experiment 2

In this experiment, the objectives of low-pass filter (LPF) are prearranged as follow: voltage gain is 20 dB, transmission bands is 30KHz., the generate ratio of resistor, capacitance, power supply, and transistor is 6:3:1:2.

A relative good circuit has been obtained after 800 1000 generations, and a perfect circuit has selected to demonstrate in Figure.2:

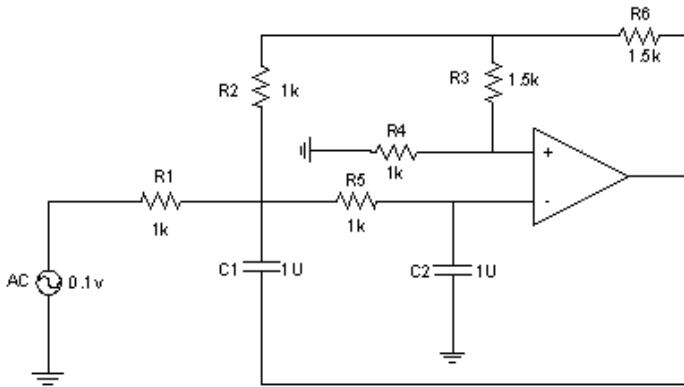


Fig. 2. The best low-pass filter structure from generation 1000

This filter allows frequency lower than 30 kHz to pass through it, but prevented higher frequencies from doing so.

3.3 Analysis

As we know that the structure and values of elements contribute to an analog circuit's function. Experiences indicate that congeneric circuits generally have the

same topology while some values of elements are different. In the experiments above, the proper topologies of a transistor amplifier and a low-pass filter were found during generation 500 600, despite that the magnification and the frequency were not consistent with the prearrangement circuits. The posterior evolutions were stress on how to adjust the values of elements in order to meet the scheduled requirements. Experiences in this paper indicated that, compare with traditional methods, this strategy shorten the period of EHW, especially in analog circuits.

4 Conclusions

In this paper, an evolution approach for designing analog circuit is proposed, which adopts a parallel evolutionary strategy that separated evolution of circuit into two parts, called structure and element value, which are organically combine by weight vectors. The experiments have indicated that parallel evolutionary strategy combining with separate fitness evaluate scheme can automatically design a circuit efficiently. Its excellence is saving time and multi-result.

Although little knowledge about circuit is required during EHW, however, the special characteristics of a circuit would consequentially improve the efficiency of EHW. So it is the main target of future researches that how to extract the characteristics of structure and element value from a preconcerted circuit to enhance the quality and to improve the efficiency of EHW. Since the strategies and operators of genetic are also important to EHW, so these strategies and operators should be explored and researched specially to ameliorate EHW.

Acknowledgement. This research is supported by the National Natural Science Foundation of China under Grant No.60473014.

References

1. Koza, J.R. Bennett, F.H. Andre, M.A. et al.: Automated synthesis of analog electrical circuits by means of genetic programming. *IEEE Trans. on Evolutionary Computation* **1**(2) (1997) 109–128
2. Koza, J.R.: *Genetic Programming: On the Programming of Computers by Means of Natural Selection*. MIT Press, Cambridge, MA (1992)
3. de Garis H.: Evolvable hardware: Genetic programming of a darwin machine. In: *Proceeding of Artificial Neural Nets and Genetic Algorithms*, Austria: Springer-Verlag (1993) 441–449
4. Cantu-Paz E.: A survey of parallel genetic algorithms. *Calculateurs parallels* **10**(2) (1998) 141–171
5. Iwata, M.: A pattern recognition system using evolvable hardware. In: *Parallel Problem Solving from Nature IV*, Springer Verlag (1996) 761–770
6. de Garis H.: An artificial brain: Atr's cam-brain project aims to build/evolve an artificial brain with a million neural net modules inside a trillion cell cellular automata machine. *New Generation Computing* **12**(2) (1994) 215–221
7. Goldberg, D.E.: *Genetic Algorithms in Search, Optimization and Machine Learning*. Addison-Wesley Publishing Company, Reading, MA (1989)