What Is beyond the RTL Horizon for Microprocessor and System Design?

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Abstract. The current state of hardware logic design and verification is discussed based on the project flow used for IBM's Power4 and Power5 projects.
The frequency and power requirements for these high-end chips constrain the logic design to a detailed RT-level in order to control physical effects. On the other hand, the complexity of the designs which embrace many speculative mechanisms to push functional performance to higher levels force an early specification of the microarchitecture with a high-level model.
A review how high-level modeling has advanced is based on the discussion which mechanisms of abstraction raise the specification above the RT-level. A critique of specification language design leads to the appeal to the formal verification community to focus efforts on the front-end of the high-level design process to help shape modeling languages with formally defined semantics that avoid the mistakes made in the past with ad-hoc language designs.

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