The Future Evolution of High-Performance Microprocessors

Norman P. Jouppi

Hewlett Packard,
Palo Alto, USA
norm.jouppi@hp.com

Abstract. The evolution of high-performance microprocessors is fast approaching several significant inflection points. First, the marginal utility of additional single-core complexity is now rapidly diminishing due to a number of factors. The increase in instructions per cycle from increases in sizes and numbers of functional units has plateaued. Meanwhile the increasing sizes of functional units and cores are beginning to have significant negative impacts on pipeline depths and the scalability of processor clock cycle times.

Second, the power of high performance microprocessors has increased rapidly over the last two decades, even as device switching energies have been significantly reduced by supply voltage scaling. However future voltage scaling will be limited by minimum practical threshold voltages. Current high-performance microprocessors are already near market limits of acceptable power dissipation. Thus scaling microprocessor performance while maintaining or even reducing overall power dissipation benefit of appreciable further voltage scaling will prove especially challenging.

In this keynote talk we will discuss these issues and propose likely scenarios for the future evolution of high-performance microprocessors.

Biography: Norman P. Jouppi is a Fellow at HP Labs in Palo Alto, California. From 1984 through 1996 he was also a consulting assistant/associate professor in the department of Electrical Engineering at Stanford University. He received his PhD in Electrical Engineering from Stanford University in 1984.

He started his contributions to high-performance microprocessors as one of the principal architects and the lead designer of the Stanford MIPS microprocessor. While at Digital Equipment Corporation's Western Research Lab he was the principal architect and lead designer of the MultiTitan and BIPS microprocessors. He has also contributed to the architecture and implementation of graphics accelerators, and has conducted extensive research in telepresence. He holds more than 25 U.S. patents and has published over 100 technical papers. He currently serves as ACM SIGARCH Chair and is a Fellow of the IEEE.

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