Simulation of Electrical and Optical Interconnections for Future VLSI ICs

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Abstract. At present, metallic interconnections become the "bottleneck" of the further progress in VLSI technology. The optical solution is considered as an alternative that could allow overcoming the limitations but its advantage should be confirmed at the level of modeling approach. The clock distribution network (CDN) that is the most representative component of the modern VLSI circuits has been used as the test circuit and its numerical models for H-tree architecture have been worked out and used. The model of the electrical CDN as well as some results of simulations presenting its expected features, also with the comparison to the results obtained for its optical counterpart are presented.

1 Introduction

The advances of semiconductor fabrication process made possible design and fabricate chips with several millions of transistors operating at a very high speed. These advances together with innovative hardware organisations of modern integrated circuits (IC's) give high performance ICs at low cost. However it becomes evident that most of the known technological capabilities will approach or reach their fundamental limits and one will require substantial changes in device technologies and structures that will become more and more 3D ones.

The progress of the VLSI systems has been driven by downsizing of their components and increasing the operating speed. In contrast to transistor scaling the interconnect scaling improves the integration density but at the cost of the degraded propagation delay and the power consumption. In the new technology, the interconnect delay dominates over logic delay even in spite when new metallization technologies such as copper or new low-k dielectrics are applied [1]. The downsizing process leads to smaller transistors characterized by smaller power consumption but the number of transistors and its density increases in such a degree that the resulting density of power dissipation becomes larger still. In spite of the multi-level (3D) design, the simultaneous growth in circuit complexity leads to larger and larger chip dimensions and the total length of interconnection lines. They are manufactured as multilevel structures, like the one shown in Fig.1, characterized by the total length reaching a few kilometers at the width below 0.3μm on the lowest level, giving a considerable contribution to the total power dissipation. As the result, in modern VLSI systems, the power dissipation increases rapidly especially in its interconnection part and in a VLSI circuit with the power dissipation of 100W [2] only the clock tree uses at least 30-50% of this power [3]. Due to natural limits in thermal management, this is a real barrier to further progress of modern VLSI systems

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and just now, it has happened that manufactures must reduce their ratings due to the thermal reason only.

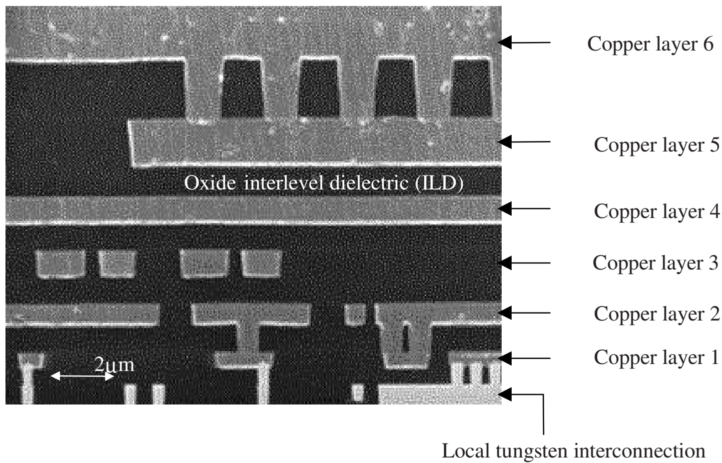

Fig. 1. Scanning electron micrographs of interconnect architecture with six levels of copper wires/vias and tungsten contacts/local interconnects

As a possible alternative that can overcome the limitation of metallic wires an optical interconnection are proposed. Applying optical interconnections to ICs has been the subject of many researches [4, 5] but no real remedy has been presented till now. It is obvious that this alternative can be acceptable only if it demonstrates significantly improved performance over the electrical solution. Unfortunately, due to the obvious reasons, the electrical metallic interconnections foreseeing by ITRS do not exist at present as well. In such a case, an approach basing on their models is the only way to evaluate and to compare the prospective features of the both solutions. This approach has been also applied in the project [6] aiming at the new optoelectronic VLSI solution with a layout covering silicon waveguides formed on the silicon chip. The clock distribution network (CDN) that is the most representative component of the modern VLSI circuits has been used as the test circuit and its model for the H-tree architecture has been worked out and used. The model of the electrical CDN and some results of simulations presenting its expected features, also with the comparison to the results obtained for its optical counterpart, are presented in the paper.

2 Clock Distribution Network (CDN)

2.1 General Description

The semiconductor technologies operate at increasingly higher speeds, and the system performance has become limited not by the delays of the individual logic elements but by the necessity to synchronize the flow of the data signals. A clock network distributes the clock signal from the clock generator, to the clock inputs of the synchronizing components. This must be done while maintaining the integrity of the

signal and minimizing such clock parameters like: the clock skew, the clock slew rate or the clock phase delay. Additionally, these objectives must be attained while minimizing the use of system resources such as the power and the area. The CDN of a modern microprocessor uses a significant fraction of the total chip power and has a substantial impact on the overall performance of the system.

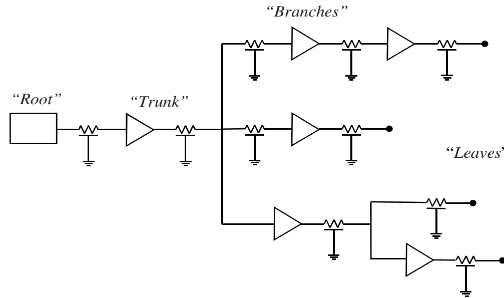

Fig. 2. The tree-like structure of the clock network

The proper generation and the distribution of the clock signal are critical for the high performance systems operating. The most common strategy for this distribution is using a tree-like structure shown in Fig.2. The clock input is connected to the "*trunk*" and the signal is subsequently split and distributed to the"*branches*" connected hierarchically that finally feed logic elements ("*leaves*"). In order to keep the quality of clock signals, the tree is completed by repeaters (buffers) built-in into the branches.

2.2 H-Tree Architecture

Fully symmetrical structures of CDN are desirable to eliminate the clock skew. The most popular solution that one considers here is the H-tree one, shown in Fig.3. That makes all the paths from the clock signal source to the clocked register being identical and therefore the clock skew is minimized. The distribution scheme repeats the H-shaped structure recursively and the lowest level of these structures covers points used to drive the local registers. Some design rules must be fulfilled to ensure the proper work of the H-tree CDN. The impedance of the branch leaving each branch point must be twice the impedance of the one providing the signal to the branch point to avoid the reflection effect at the branch point [7], and appropriate buffers must be built-in into the H-tree branches. The both demands have been met in the worked out model.

3 Model of Electrical H-Tree CDN

3.1 General Description

The most recent microprocessors have as many as seven metal layers [2], while the ITRS predicts the use of up to 10 levels of wiring for the 45nm technology node in

2010 at up to $2x10^9$ transistors per chip, and clock frequencies up to 10 GHz. Coping with the analyze of electrical interconnections under the above conditions is a task that requires an adequate tool allowing to investigate the signal propagation in the considered system, and dedicated numerical models seem to meet this demand. Such a model for H-tree CDN has been worked out in a form of ICAL software package. It allows designing any H-tree structure for any technology level predicted by ITRS, extracting the electric parameters from technology data both for transmission lines and necessary buffers, and creating an equivalent circuit model presented in a form of SPICE netlist useful in further circuit simulations.

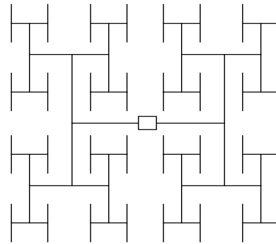

Fig. 3. The H-tree topology

3.2 Transmission Line Model

The interconnection system in a VLSI chip covers two power lines and one signal line as shown in Fig.4. The technology used to its realization allows considering the power lines as a meshed network that plays the role of distributed current sources supplying all electronic elements equally. The signal line must, however, be considered as a transmission line coupling buffers sketched as CMOS inverters, and characterized by its resistivity R, inductivity L and capacity C that can be used to model it as an RC or RLC transmission line shown in Fig.4a. When such models are created for CDN transmission lines, the specificity in realizing them consists in shielding the signal wires at the sides by power, and ground lines as shown in Fig.4b.

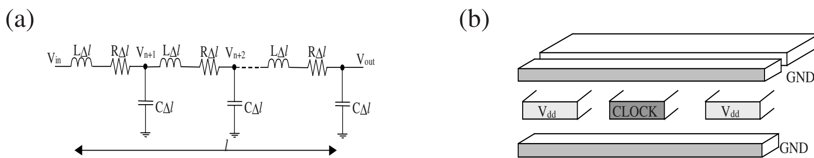

Fig. 4. Distributed RLC interconnection model (a) and clock wire shielding (b)

Interconnection resistance. The interconnection resistance per unit length, R_o, is generally determined by (1) where ρ - resistivity of the metal layer, W - width of the wire and T - its thickness. At large signal frequencies, the resistance can by changed by the skin effect and such a possibility is introduced into ICAL. It takes place when the skin effect depth δ is smaller than the wire dimension, what can, however, happen

very seldom in considered CDN systems since δ=0.7μm for the maximal ITRS frequency, f=10GHz.

$$R_o = \frac{\rho}{W*T} \tag{1}$$

Interconnection capacitance. Parasitic capacitances associated with the interconnection lines are shown schematically in Fig.5. They have become the primary factors in the evolution of the very high speed integrated circuit technology, their evaluation is not a trivial task and has been the subject of many investigations [8-10]. To get an accurate interconnection capacitance, 2D or 3D electric field simulation in the whole interconnection system should be applied. It is, however, such a huge task that in real applications approximate approaches have been used only. They treat the total interconnection capacitance as a sum of a few different capacitances resulting from the particular design and differ the way of the components capacitances identification.

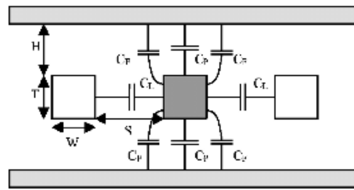

Fig. 5. Interconnect capacitance components: C_P - parallel plate capacitance component, C_F - fringing field component, C_L - lateral coupling capacitance component

The most popular approaches were proposed by Saravat [11], Sakurai [12], Chern [13] and Wong [14] and their application in ICAL has been considered. Since each of them gives another evaluation of the total capacitance C_{tot} for designs predicted by ITRS and their experimental verification is impossible, the numerical simulation has been used to recognize which one of them could be used. In this goal the software package OPERA [15] using finite element techniques to solve the Maxwell equations has been used to analyze electric field in 2D domain shown in Fig.4b. The electric field distributions, like the one in Fig.6, were used to calculate the real values of C_{tot} that were compared to the evaluations obtained by means of tested approaches The comparison showed that only for the Chern approach the discrepancy was lower than 7% over a wide range of ITRS parameters whereas it was much larger for the others. The Chern approach has been chosen for ICAL package.

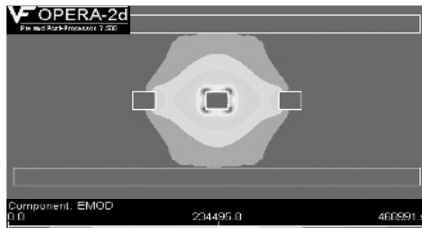

Fig. 6. Interconnect structure used in numerical capacitance calculation

Interconnection inductance. In today's VLSI circuits, the inductance starts to become significant due to longer metal interconnections, the reduction in wire resistances and the higher operation frequency. The analytical expressions (2) and (3) have been obtained [16] for partial self and mutual inductances, respectively, under the assumption of uniform current distribution and rectangular shape of wires shown in Fig.7.

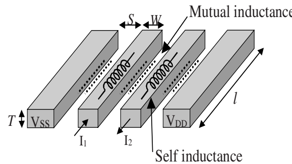

Fig. 7. On-chip interconnection inductance

$$L = \frac{\mu_o l}{2\pi}\left[\ln\left(\frac{2l}{W+T}\right) + 0.5 + \frac{0.2235(W+T)}{l}\right] \quad (2)$$

$$M = \frac{\mu_o l}{2\pi}\left[\ln\left(\frac{2l}{S}\right) - 1 + \frac{S}{l}\right] \quad (3))$$

3.3 Buffer Model

The accurate characterization of the MOSFET transistor is crucial for any high speed digital integrated circuit analysis and design. In order to calculate the clock path delay, buffers incorporated into ICAL program are modeled by an equivalent circuit shown in Fig.8a (where D_{Inv} is the buffer internal delay, R_{Inv} is the buffer output resistance, C_{in} is the buffer input capacitance and V is the logic swing on the clock lines) and by the transistor level model shown in Fig.8b. Taking into account the demands resulting from the technologies predicted by ITRS, the Berkeley BSIM3v3 and BSIM4 MOS models were used in the transistor level model.

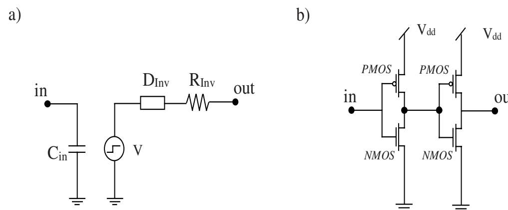

Fig. 8. Models of buffer devices. a) Equivalent circuits. b) Transistor level model

4 Results of Simulation

The majority of investigations have been performed for 128 and 256 symmetrical global H-trees manufactured on 300-450 mm^2 chips depending on the ITRS demands for the assumed technology. Some of these results are collected in Fig 9-12.

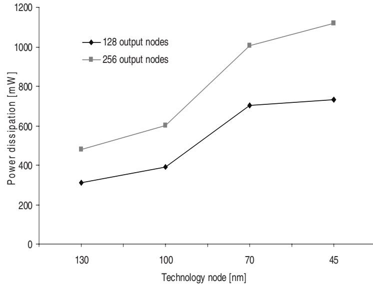

Fig. 9. Power dissipated in electrical H-trees vs. technology

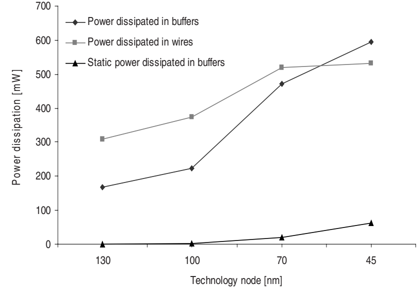

Fig. 10. Power budget in the electrical H-tree networks at 256 output nodes

Fig.9 shows the electrical power consumption in the global H-trees versus technology node, and the operating frequencies for considered systems are (in GHz/technology): 1.6/130nm, 3/100nm, (5.6 and 11.5)/(70nm and 45nm). It is obvious that the total power consumption in electrical clock distribution network tends to grow despite technology improvements. Fig.10 shows the power dissipated by buffers and wires in for various technology nodes. It shows that along with technology scaling the contribution of the power consumed by buffers to the total power consumption tends to grow, and for the 45nm technology it will be even bigger than the power consumed by wires due to increasingly large number of repeaters used in clock distribution systems. Fig.11 shows the dependence of the power consumption for both electrical and optical CDN's on the frequency for 70nm technology node. Whereas the power consumption in the electrical system increases rapidly with the increase of the clock frequency, in the optical system it remains almost on the same level. In Fig.12 the power consumption is plotted as a function of the chip width for f=5.6GHz and 70nm technology node rules. In opposite to the optical CDN, in the electrical one, the power consumption increases drastically when the die size increases.

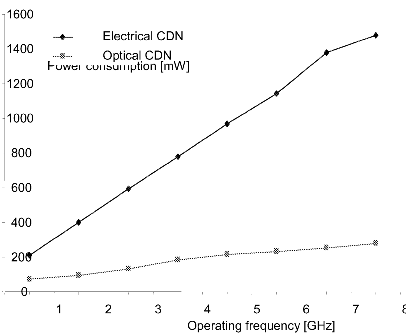

Fig. 11. Power consumption in optical and electrical CDN's versus operating frequency at 256 output nodes

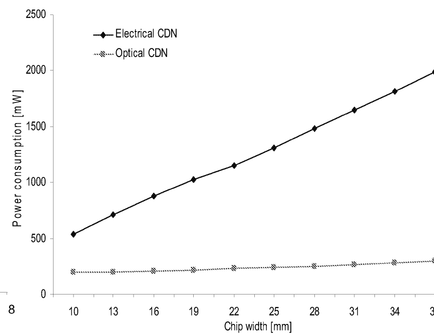

Fig. 12. Power consumption in optical and electrical CDN's versus chip width. at 256 output nodes

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