Statistical Evaluation of Digital Techniques for $\Sigma\Delta$ ADC BIST

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Abstract. Digital techniques for an embedded dynamic test of $\Sigma\Delta$ ADCs have been recently presented in the literature. These techniques are based on the use of $\Sigma\Delta$ streams for the stimulation of the ADC. Binary and ternary test stimuli have been proposed. In this chapter, we aim at the validation of these embedded test techniques, comparing the results obtained with the different types of digital stimuli with a standard high-resolution analog sinusoidal stimulus. This validation is done in terms of the expected yield loss and test escapes of the proposed embedded techniques. However, performing this validation at the design stage demands extensive computational resources, which may render electrical simulations infeasible. Thus, we propose an advanced simulation framework for this validation. The proposed simulation strategy relies on a combination of transistor-level simulations, behavioral simulations, and statistical tools.

1 Introduction

The standard approach for characterizing the dynamic performance of an analog-to-digital converter (ADC), i.e. signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), etc., requires the application of a full-scale sinusoidal analog test stimulus at the input of the ADC and the collection of a high number of output samples to accurately compute the spectrum of the ADC response [1,2]. The resolution of the sinusoidal analog test stimulus is required to be at least two or three bits above the resolution of the ADC, such that the noise and distortion at the output are predominantly due to the ADC. The test resources for generating the test stimulus and for storing and processing the digital samples of the ADC response can be found in any modern Automatic Test Equipment (ATE). Yet, a built-in test approach where test stimulus generation and response evaluation are instead implemented on-chip would greatly reduce test costs, since the ATE requirements would be relaxed and the test throughput would be increased. However, implementing these test resources on-chip with low overhead circuitry remains a challenging task. Especially, the on-chip generation of a high-resolution analog sinusoidal test stimulus is extremely challenging and has led to the search

L. Claesen et al. (Eds.): VLSI-SoC 2014, IFIP AICT 464, pp. 129–148, 2015.
DOI: 10.1007/978-3-319-25279-7_8

for equivalent digital techniques. $\Sigma\Delta$ ADCs in particular offer this possibility and are the focus of this chapter.

In this line, an idea that has been thoroughly explored in the literature is the use of $\Sigma\Delta$ digital bitstreams to encode a high-resolution analog sinusoidal test stimulus. As it is schematically depicted in Fig. 1, the starting point is to use an ideal $\Sigma\Delta$ modulator in software that converts a high-resolution analog sinusoid to a bitstream [6]. The bitstream is divided in sub-bitstreams of length N and the sub-bitstream with the highest resolution (i.e. highest SNR, SNDR, etc.) is selected to be periodically reproduced through a circular shift register. Bitstreams can also be generated by on-chip digital oscillators, but their design is not as straightforward [9,10]. The bitstream can be converted to a high-resolution analog sinusoid by passing it through a 1-bit digital-to-analog converter (DAC), which could simply be a digital buffer, followed by a low-pass filter to remove the quantization noise. Although this solution is applicable for a built-off test where the 1-bit DAC and the low-pass filter are placed on the load board [12], it is not applicable for a built-in test since the low-pass filter is far more complex than the $\Sigma\Delta$ modulator itself [13].

Interestingly, in the case of switched-capacitor (SC) $\Sigma\Delta$ ADCs, the bitstream can be fed directly into the modulator by adding simple circuitry at its input [7,17,18]. Typically, a 1-bit DAC is merged into the first integrator in the $\Sigma\Delta$ modulator, and used to convert the bitstream to the analog reference voltages of the modulator. Figure 2 shows an efficient implementation of this approach into a generic SC integrator. As it can be seen, the injection of the $\Sigma\Delta$ bitstream only requires the addition of four switches, which is a negligible modification in the overall design of the modulator.

However, the direct application of the bitstream to the input of the ADC will overload the modulator, unless the reference voltages of the 1-bit DAC are

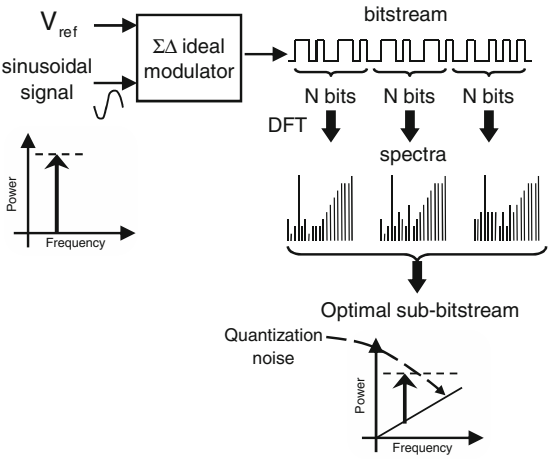

Fig. 1. Generation of optimized $\Sigma\Delta$ digital bitstreams.

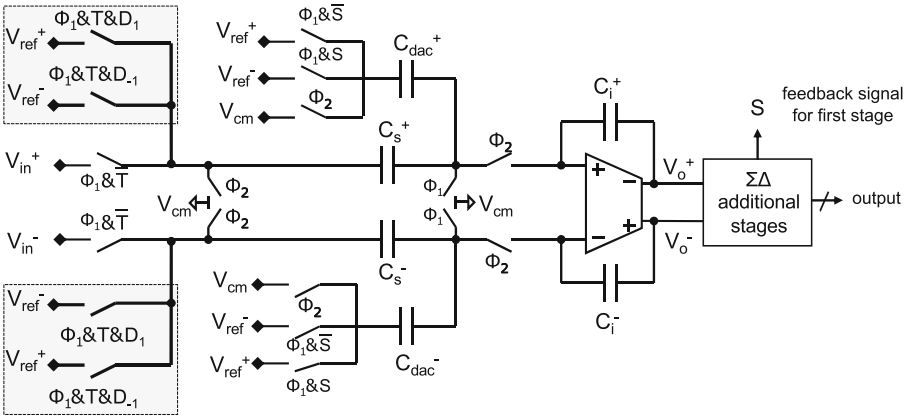

Fig. 2. Injection of binary stimulus $\{D_{-1}, D_1\}$ into the first stage of a generic switched-capacitor $\Sigma\Delta$ modulator.

adequately attenuated. Unfortunately, by attenuating these reference voltages we also scale down the amplitude of the encoded sinusoid. The maximum amplitude that can be encoded in the bitstream is in fact less than the actual dynamic range of the ADC and, thereby, we do not test the dynamic performances of the ADC at full scale. Especially for measuring SNDR, the amplitude of the test stimulus has to be as close as possible to full scale such that the harmonic distortion introduced by the ADC under test is amply manifested [15].

A solution to this problem has been proposed in [8]. More specifically, the input switched-capacitor network of the modulator is reconfigured in test mode in such a way that it accepts multiple bitstreams delayed from each other. This reconfiguration is shown to attenuate the noise power of the test stimulus, thus the modulator starts overloading for a test stimulus with a much higher amplitude than before. However, this comes at the expense of modifying significantly the input stage of the modulator.

An elegant approach to overcome this issue was presented in [3]. A test stimulus is encoded in a ternary stream that is composed of three levels $\{-1, 0, 1\}$. The ternary stream is converted to a three-level analog signal directly at the input stage of the modulator. The conversion does not require reconfiguration of the input stage and is achieved through the addition of only four switches, that is, just as in the case of applying a digital bitstream. The proposed approach presents minimal overhead and allows measuring SNDR for amplitudes close to full scale.

In this chapter, we present a review of dynamic testing of $\Sigma\Delta$ ADCs based on a ternary test stimulus and we develop a simulation framework to validate this test approach. This chapter extends and improves the techniques and strategies previously presented by the authors in [4]. The proposed simulation framework allows us to compare the ternary test stimulus against the bitstream and high-resolution sinusoidal test stimuli, in order to show its feasibility and

accuracy. Our simulation framework relies on a combination of transistor-level and behavioral-level simulations to generate instances of the $\Sigma\Delta$ ADC that span the whole feasible design space. In this way, we are able to examine the correlation between the test decisions obtained by applying the aforementioned three test stimuli.

The rest of the chapter is organized as follows. Section 2 presents our strategy for dynamic test of $\Sigma\Delta$ ADCs based on a ternary test stimulus. Section 3 discusses an efficient on-chip implementation. Section 4 describes our proposed simulation framework for validating our test strategy, while Sect. 5 demonstrates its application on a second-order SC $\Sigma\Delta$ ADC that has been implemented in a 130 nm CMOS technology. Finally, Sect. 6 concludes the chapter.

2 Dynamic Test of $\Sigma\Delta$ ADCs Using Digital Ternary Stimuli

Our test approach is a fully-digital, low-cost BIST strategy for measuring the Signal-to-Noise and Distortion Ratio (SNDR) of $\Sigma\Delta$ ADCs, originally proposed in [3,18]. Figure 3 shows the general block diagram of the BIST strategy. The BIST circuitry is mainly composed of two digital blocks, namely the Stimulus Generator, and Response Analyzer. During test mode, the $\Sigma\Delta$ ADC under test is disconnected from the main signal path and is connected to the Stimulus Generator and the Response Analyzer. The Stimulus Generator provides an optimized digital ternary stimulus to the input whereas the Response Analyzer computes the SNDR based on a simplification of the sine-wave fitting algorithm. In the following subsections, we discuss the theoretical basis of the ternary stimulus and its optimization, as well as the theoretical basis of the response analysis strategy. An efficient on-chip implementation is discussed in Sect. 3.

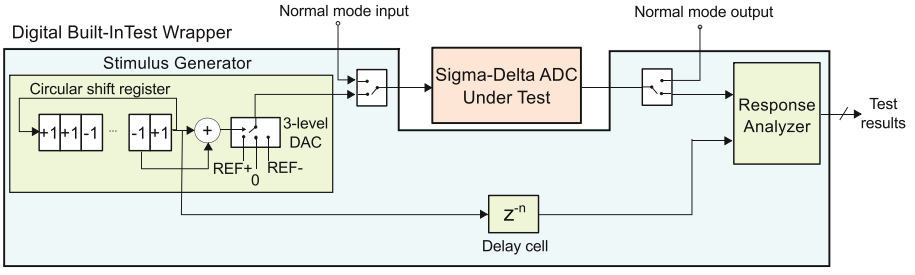

Fig. 3. General block diagram of the BIST strategy for $\Sigma\Delta$ ADCs.

2.1 Ternary Stimulus: Theoretical Basis

Our test strategy for the dynamic test of $\Sigma\Delta$ ADCs is based on the injection of a high-linearity ternary stimulus that is composed of three levels $\{-1, 0, 1\}$ at

the input of the modulator of the $\Sigma\Delta$ ADC under test. The ternary stimulus is generated in the digital domain by adding a $\Sigma\Delta$ encoded binary bitstream with a delayed version of itself, as shown in Fig. 4.

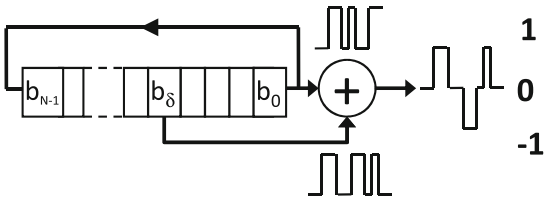

Fig. 4. Ternary stream construction.

From a spectral point of view, the Discrete Fourier Transform (DFT) of a length-N bitstream $\{b_0, \cdots, b_{N-1}\}$ is given by

$$B(k) = \sum_{n=0}^{N-1} b_n \cdot e^{-j\frac{2\pi \cdot n}{N}k}, \quad k = 0, \cdots, N-1. \tag{1}$$

The N periodic extension leads to a spectrum made by N lines located at $f_k = kf_s/N$, where f_s is the sampling frequency. The DFT of the circular-shifted bitstream delayed by δ samples $\{b_\delta, \cdots, b_{N-1}, b_0, \cdots, b_{\delta-1}\}$ is obtained by applying the time shift theorem to (1)

$$B_\delta(k) = B(k) \cdot e^{-j\frac{2\pi}{N}\delta k}, \quad k, \delta = 0, \cdots, N-1. \tag{2}$$

The DFT of the ternary stream is then obtained by averaging the DFT of the original bitstream and the DFT of the circular-shifted version of it and by using the linearity property of the DFT

$$T(k) = \frac{B(k)}{2}\left(1 + e^{-j\frac{2\pi}{N}\delta k}\right), \quad k, \delta = 0, \cdots, N-1. \tag{3}$$

The Power Spectral Density (PSD) of the bitstream and the ternary stream are given by

$$S_B(k) = \|B(k)\|^2 \tag{4}$$

$$S_T(k) = S_B(k) \cdot cos^2\left(\frac{\pi k\delta}{N}\right) \tag{5}$$

$$k, \delta = 0, \cdots, N-1.$$

Therefore, for $\delta = 1, \cdots, N-1$, $k = 0, \cdots, N-1$, the amplitude of the spectra of the ternary stream is lower than the amplitude of the spectra of the bitstream, i.e. $S_T(k) < S_B(k)$, and the cumulative PSD of the ternary stream $Pq_T(n) = \sum_{k=2}^{n} S_T(k)$ is less than the cumulative PSD of the bitstream

$Pq_B(n) = \sum_{k=2}^{n} S_B(k)$, i.e. $Pq_T(n) < Pq_B(n)$, $n = 2, \cdots, N-1$. This is shown graphically in Fig. 5 for $\delta = 1$. As it can be observed, the spectra of the ternary stream presents a high frequency filter behaviour and the quantization noise power of the ternary stream is about 6 dB less than the quantization noise power of the bitstream. In other words, the ternary stream overloads less the modulator compared to the bitstream and, thereby, offers the possibility of testing the $\Sigma\Delta$ ADC closer to full scale.

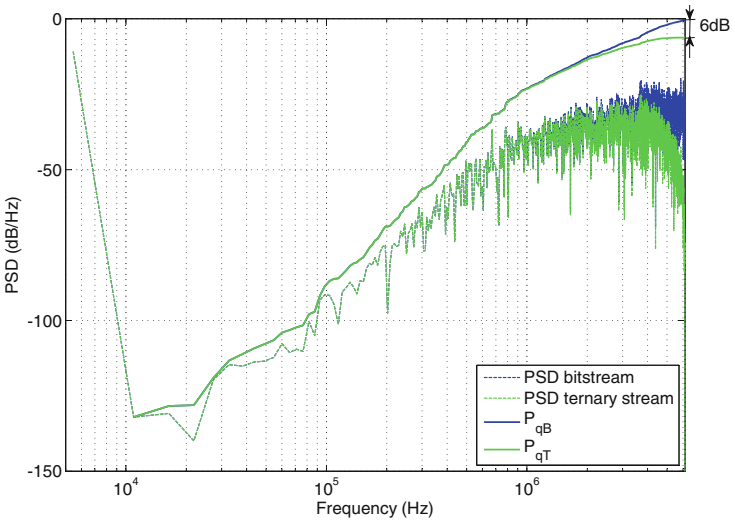

Fig. 5. Power spectral density and cumulative power spectral density of a bitstream and a ternary stream for $\delta = 1$.

The fundamental of the ternary stream is given from (3) for $k = 1$

$$\begin{aligned} T(1) &= \frac{B(1)}{2} \cdot \left(1 + e^{-j\frac{2\pi}{N}\delta}\right) \\ &= B(1) \cdot cos\left(\frac{\pi \cdot \delta}{N}\right) \cdot e^{-j\frac{\pi}{N}\delta}, \\ &\delta = 0, \cdots, N-1. \end{aligned} \tag{6}$$

If we denote by A_T and Φ_T the amplitude and the phase of the fundamental of the ternary stream and by A_B and Φ_B the amplitude and the phase of the fundamental of the bitstream, then from (6)

$$A_T = A_B \cdot |cos\left(\frac{\pi \cdot \delta}{N}\right)| \tag{7}$$

$$\Phi_T - \Phi_B = -\frac{\pi}{N}\delta \qquad \delta = 0, \cdots, N-1. \tag{8}$$

Therefore, when $\delta \ll N$, $A_T \approx A_B$ and $\Phi_T \approx \Phi_B$, i.e. the amplitude and the phase of the fundamental encoded in the ternary stream are practically the same with the amplitude and the phase of the fundamental encoded in the bitstream. As δ increases, A_T decreases with respect to A_B and the phase difference $\Phi_T - \Phi_B$ moves away from zero. These relationships are plotted in Fig. 6.

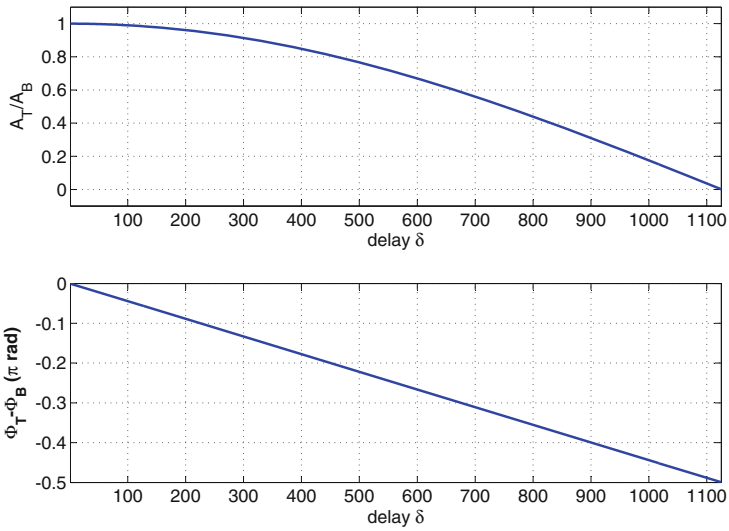

Fig. 6. Encoded signal amplitude and phase versus delay δ (for $\delta = 1$ to N/2).

2.2 Ternary Stimulus Optimization

For a meaningful dynamic test, the in-band noise and harmonic distortion of the ternary test stimulus have to be smaller than the noise and distortion originated by the $\Sigma\Delta$ ADC under test. Typically, the SNDR of the test stimulus should be at least 3 effective number of bits (ENOB) higher than the SNDR specification of the $\Sigma\Delta$ ADC. Moreover, the power of the test stimulus has to be as small as possible to avoid overloading the $\Sigma\Delta$ modulator. The ternary stimulus has to be optimized so as to fulfill these requirements.

The spectral quality of the ternary stimulus is defined by two parameters: the initial bitstream and the delay parameter δ. Concerning the initial bitstream, our optimization loop simulates an ideal $\Sigma\Delta$ modulator of one order higher than the $\Sigma\Delta$ modulator under test using a pure sinusoidal input signal of an amplitude A_T. From the output of this ideal $\Sigma\Delta$ modulator, the algorithm selects several bitstreams of length N equal to the period of the input signal and it records their total power $P_B = Pq_B(N-1)$. Next, for each bitstream, it computes the SNDR and the total power of the resulting ternary stream $P_T = Pq_T(N-1)$ for different values of δ. The objective of the optimization loop is to select a

ternary stream that has a SNDR larger than the SNDR specification of the $\Sigma\Delta$ modulator by at least 3 ENOB and a low power P_T or, equivalently, a large ratio P_B/P_T.

As an example of the described optimization procedure, Fig. 7 plots the SNDR of the ternary stream versus the ratio P_B/P_T for different initial bitstreams of length $N = 2252$, extracted from an ideal third-order $\Sigma\Delta$ modulator excited by a pure sinusoid with amplitude $A_T = -8$ dBFS. Five different values of δ were considered in the optimization. For a given δ, the large SNDR variations stem from using different initial bitstreams to generate the ternary stream. For a given initial bitstream, we obtain different ratios P_B/P_T by varying δ. It can be seen that the highest P_B/P_T is achieved for $\delta = 1$. In particular, for this choice of δ, the total power of the ternary test stimulus is 5 times lower than the total power of the bitstream from which it is generated. Furthermore, from Fig. 8, which is a zoom onto the upper right corner of Fig. 7, it can be seen that for a given δ the highest SNDR does not necessarily correspond to the best possible ratio P_B/P_T. Thus, amongst the bitstreams that result in a ternary stream with an SNDR at least 3 ENOB higher than the SNDR specification of the $\Sigma\Delta$ modulator under test, we select the sequence that has the best ratio P_B/P_T. Assuming an SNDR specification of 106 dB, the optimal bitstream circled in Fig. 8 has an SNDR of 109.5 dB with a ratio P_B/P_T of around 5.25.

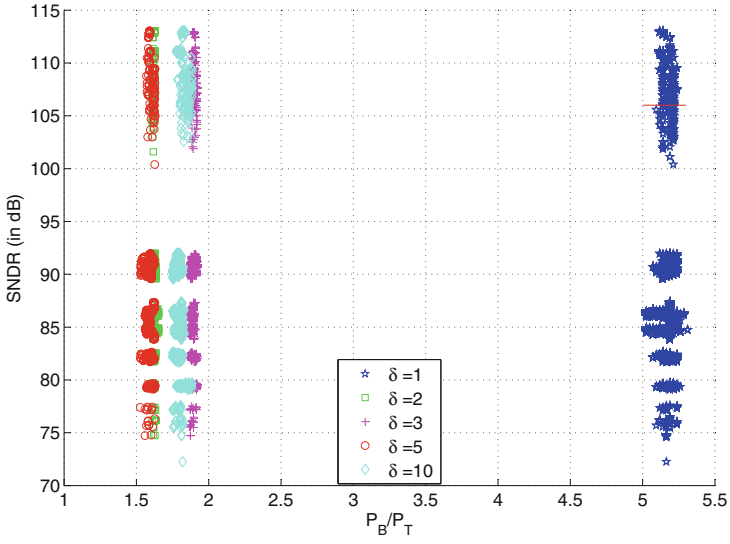

Fig. 7. SNDR of the ternary stream versus the power ratio P_B/P_T as a function of the delay parameter δ.

Finally, this algorithm is repeated for different input signal amplitudes A_T, in order to generate optimized test stimuli that cover the whole dynamic range

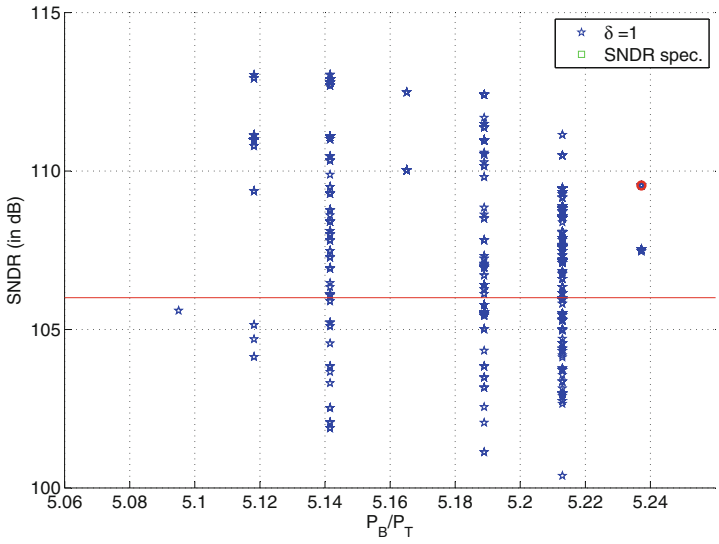

Fig. 8. Selection of a ternary stream that has an appropriate SNDR.

of the $\Sigma\Delta$ ADC under test. Figure 9 plots the SNDR of the ternary stream as a function of the input signal amplitude A_T. In all cases, the SNDR of the ternary stream exceeds the SNDR specification of the $\Sigma\Delta$ modulator by more than 3 ENOB. A ternary stream that encodes a sinusoid with full scale amplitude cannot be obtained since the bitstream generator will be overloaded. However, this is not a concern since the $\Sigma\Delta$ modulator under test itself is overloaded for amplitudes very close to the full scale.

2.3 Response Evaluation: Theoretical Basis

The analysis of the ADC response is performed by a simplified version of the sine-wave fitting algorithm. This simplification is based on the fact that our test stimulus and reference signal have the same frequency and they are completely synchronized, which saves us from computing the phase of the test response. This synchronization between the response and reference signals is easily achieved in the digital domain by designing the delay cell in Fig. 3 to match the delay introduced by the $\Sigma\Delta$ modulator. Next, we describe in detail the proposed response evaluation algorithm.

In a first step, the algorithm computes the DC component of the response signal as

$$DC = \frac{1}{N}\sum_{i=1}^{N} S_{out}(i), \tag{9}$$

where $S_{out}(i)$ are the samples of the ADC output (i.e. the signal under evaluation) and N is the number of samples considered in the evaluation.

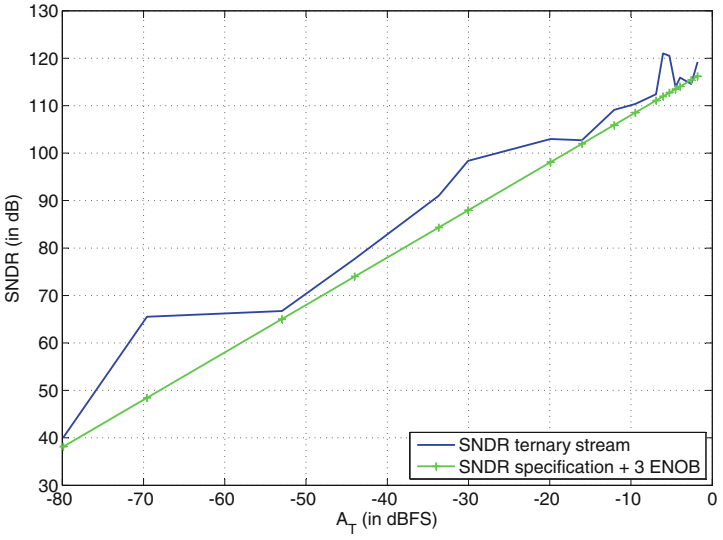

Fig. 9. SNDR of the optimized ternary stream for different input signal amplitudes A_T.

In a second step, the algorithm computes the point-to-point correlation of the response and reference signals as

$$Correl = \sum_{i=1}^{N} S_{out}(i) S_{ref}(i), \tag{10}$$

where $S_{ref}(i)$ are the samples of the reference signal.

The amplitude of the response signal is related to the computed correlation as

$$A = \frac{2}{N A_{ref}} Correl, \tag{11}$$

where A_{ref} is the amplitude of the reference signal, which is known *a priori*. Once the amplitude of the response signal has been computed, the algorithm continues by adjusting the reference signal to the amplitude and DC values obtained

$$S_{ref,adj}(i) = \frac{A}{A_{ref}} S_{ref}(i) + DC. \tag{12}$$

Finally, the algorithm computes the noise and distortion power in the response signal, denoted by P_{error}, by comparing the samples of the ADC output with the samples of the adjusted reference signal

$$P_{error} = \frac{1}{N} \sum_{i=1}^{N} \left(S_{out}(i) - S_{ref,adj}(i) \right)^2 . \tag{13}$$

With the obtained P_{error} it is straightforward to compute the SNDR of the response signal as

$$SNDR = 10 \log \frac{A^2/2}{P_{error}}. \tag{14}$$

Finally, by performing a comparison with a preloaded threshold, the BIST can provide a go/no-go output signal. Specifically, from (14)

$$Go/No\text{-}Go = \begin{cases} 1, & \text{if } \frac{A^2}{2} \geqslant P_{error} 10^{SNDR_{spec}/10} \\ 0, & \text{if } \frac{A^2}{2} < P_{error} 10^{SNDR_{spec}/10} \end{cases} \tag{15}$$

where the threshold value $SNDR_{spec}$ is the actual SNDR specification limit.

3 Efficient On-chip Implementation

The ternary stimulus can be efficiently generated on-chip while the response analysis is a purely digital algorithm, making the proposed strategy overall very suitable for a full BIST implementation, as illustrated in the general block diagram in Fig. 3.

Specifically, the ternary stimulus generator, although it is mostly digital, requires the introduction of a mixed-signal element, i.e. a 3-level DAC, to interface the digital ternary stimulus to the analog $\Sigma\Delta$ modulator. Figure 10 shows two different possible implementations for the digital part of the ternary stimulus generator. Figure 10(a) shows a strategy where the ATE is occupied for a

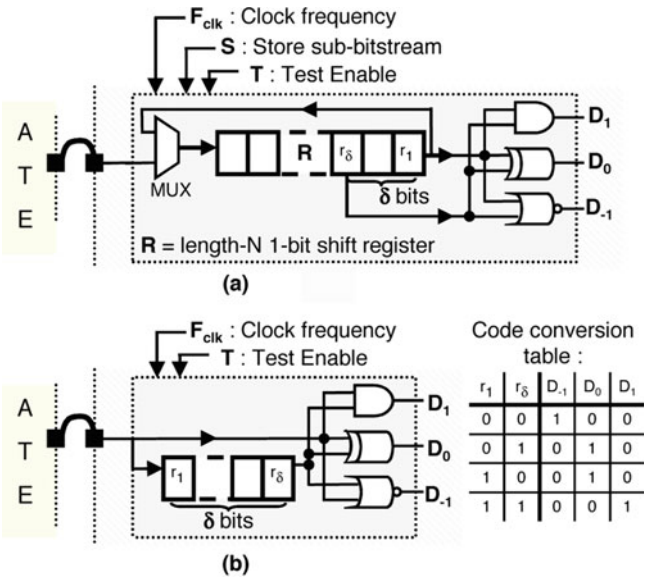

Fig. 10. On-chip generation of the ternary stream.

very small time interval to store in an on-chip shift register the length-N bitstream. During the testing phase, the bitstream circulates in the shift register and three logic gates are used to generate $\{D_{-1}, D_0, D_1\}$ that correspond to the three states $\{-1, 0, 1\}$ of the ternary stream. Another possibility, which incurs a lower area overhead, is to provide periodically the bitstream directly from the ATE, as shown in Fig. 10(b). This last implementation is attractive in the case where the bitstream can be generated on-chip using a digital resonator.

Concerning the injection of the digital ternary stimulus into the analog input of the modulator, the necessary Digital-to-Analog interface can be easily merged into the input section of a SC $\Sigma\Delta$ modulator. Figure 11 shows an implementation example for a generic fully-differential SC $\Sigma\Delta$ modulator. This implementation exploits the inherent linearity of 1-bit DACs built by two switches to perform the conversion. The test is enabled for $T = 1$. The states 1 and -1 are converted to a positive ΔV_{ref} and a negative $-\Delta V_{ref}$ differential voltage, respectively. To preserve the linearity of the test stimulus, the 0 state must correspond to the middle point between ΔV_{ref} and $-\Delta V_{ref}$, that is, the null differential voltage. Thus, the state 0 must be implemented by generating a null differential voltage at the input of the sampling capacitors, which corresponds to fully discharging the sampling capacitors. This can be achieved by switching the sampling capacitors to the common-mode voltage V_{cm} during the sampling phase, as shown in Fig. 11. Notice that the injection of the 0 state makes use of existing switches while the injection of the 1 and -1 states requires the addition of only four additional switches that are in the highlighted area. Finally, concerning the response analysis algorithm, its fully-digital implementation can be synthesized using standard digital design techniques and is out of the scope of this chapter.

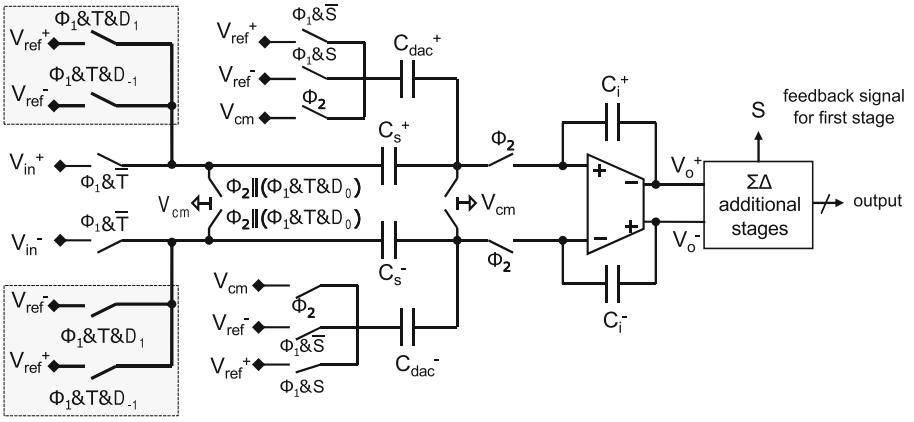

Fig. 11. Injection of the ternary stream $\{D_{-1}, D_0, D_1\}$ at the input of a SC $\Sigma\Delta$ modulator.

4 Simulation Framework

A key point for proving the feasibility of any embedded test strategy is to assess the resultant yield loss and test escapes. Yield loss is defined as the probability that a circuit will fail the test given that it is functional and test escape is defined as the probability that a circuit will pass the test given that it is faulty. In our analysis, we exclude catastrophic defects in the calculation of test escape since they are easily detectable and we focus exclusively on process variations which can bring the circuit outside the nominal specification range and are much more challenging to detect. In this case, we refer to parametric faults. The validation step has to be performed before deploying the proposed test technique into production, and, thereby, needs to rely necessarily on Monte Carlo simulations.

However, transistor-level Monte Carlo simulations may imply an important computational effort, depending on how fast the particular circuit under test can be simulated and also on the yield of the fabrication process. If the fabrication process has a natural parametric fault level in the range of a few hundreds of ppms (parts per million), then a small-scale Monte Carlo simulation will produce very few samples, if any at all, in the pass-fail boundary. In this case, a correct estimation of the test metrics, such as yield loss and parametric test escape, would require a prohibitively large number of Monte Carlo runs. Furthermore, regarding the case of $\Sigma\Delta$ ADCs, a single transistor-level simulation to compute the SNDR performance with an acceptable level of confidence could take days to complete. In short, direct transistor-level Monte Carlo simulations for estimating test metrics are computationally infeasible for our case study. Next, we propose a simulation framework for validation of the proposed test technique that overcomes this issue by relying in a combination of transistor-level simulations, behavioral-level simulations, and statistical tools.

The proposed simulation framework is schematically depicted in Fig. 12. Instead of simulating the complete $\Sigma\Delta$ ADC, in a first step we are going to break down the circuit into different building blocks. These building blocks are comparatively much smaller than the complete circuit and can be efficiently simulated at transistor-level. We then carry out an initial set of Monte Carlo runs for each building block separately, but using the same seed for each batch of simulations, such that the same sequence of process parameter vectors (e.g. the same netlists) are simulated for each batch of simulations. These simulations are, in any case, performed at the design stage by the designers to evaluate the robustness of the design, so they do not increase the design effort. The set of performances extracted from these simulations are used as behavioral parameters in a high-level behavioral model of the complete circuit. This way, we can efficiently estimate the effect of process parameter variations on the performance of the complete circuit.

The initial number of Monte Carlo runs needs to be low enough to keep the simulation time constrained, so it is unlikely that these simulations yield any samples of the complete circuit that have an SNDR close to the specification limit. In fact, it is likely that the majority of the samples will have an SNDR around the nominal value. To produce extreme variations that can bring

the circuit out of specification, we propose to use a classical design of experiment technique in the behavioral parameter space. Specifically, we perform a Latin-Hypercube Sampling (LHS) in order to evenly cover the complete feasible behavioral parameter space. This way, we can easily draw vectors of behavioral parameters that correspond to extreme process parameter variations. By feeding these extreme behavioral parameters to the behavioral model, we can then produce extreme instances of the complete circuit that have an SNDR far from the nominal value.

5 Case Study

The following subsections describe the simulation framework and the obtained simulation results for a second-order SC $\Sigma\Delta$ modulator that has been implemented in a 130 nm CMOS technology [18]. This modulator is designed for audio ADC applications that must have 16 bits of resolution or, equivalently, an output SNDR of at least 96 dB.

5.1 Behavioral Model

$\Sigma\Delta$ ADCs are usually simulated by means of a behavioral model, since one transistor-level simulation may take several days to complete. The proposed behavioral model captures the main non-idealities of the individual sub-blocks composing the ADC by performing transistor-level simulations of the isolated blocks. Given that the decimation filter is not affected by parametric deviations since it is a digital circuit operating at moderate frequencies, only the non-idealities of the blocks of the $\Sigma\Delta$ modulator are considered. For the same reason, we do not include in this case study the on-chip response analysis block. Being a purely digital algorithm, it has been emulated in software. We consider the following non-idealities in the first integrator stage: finite amplifier open-loop gain and unity gain frequency, limited slew-rate, output saturation levels, kT/C noise, amplifier thermal noise, and clock jitter. Most non-idealities in the second integrator stage are of much less relative importance since they are attenuated due to the noise shaping. The only non-ideality that we consider for this stage is the output saturation levels. Finally, we consider the offset of the output comparator. The behavioral model derivation is explained in detail in [5,11,16]. The complete behavioral model, depicted in Fig. 13, is built and simulated in Matlab Simulink®. A single behavioral simulation to calculate SNDR with an accuracy of 0.1 dB lasts about 10 s on an Intel Core2 2.40 GHz PC.

5.2 Fault-Free Case

A vector of nominal behavioral parameters is extracted from transistor-level simulations of the sub-blocks that synthesize the $\Sigma\Delta$ modulator. The behavioral model is simulated for three different test stimuli: an ideal analog sinusoid that corresponds to a standard test, an optimized ternary stream where the ideal

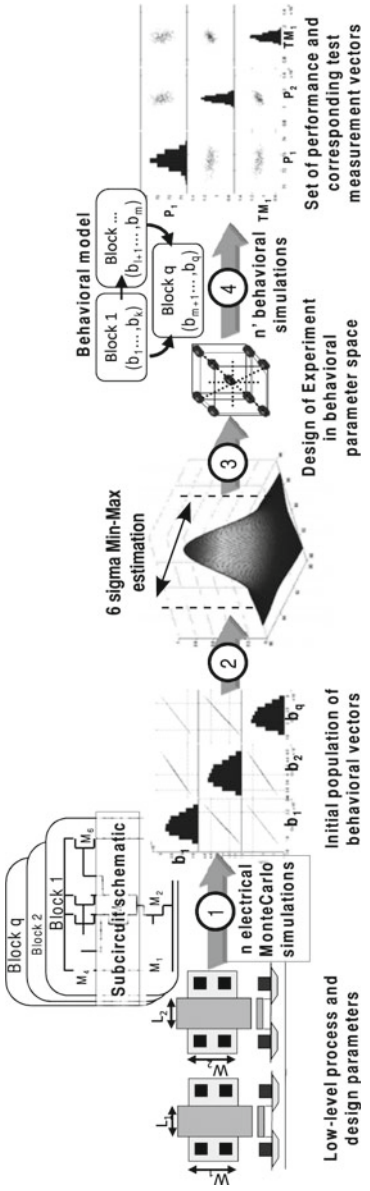

Fig. 12. Simulation framework.

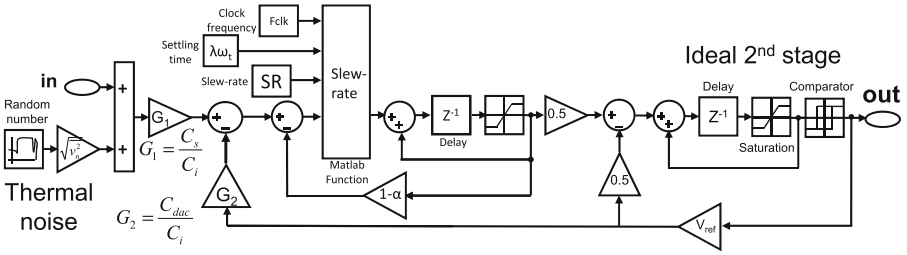

Fig. 13. Behavioral model for the second-order switched-capacitor $\Sigma\Delta$ modulator under study.

analog sinusoid serves as the input to the ideal $\Sigma\Delta$ modulator in software, and the selected bitstream from the output of the ideal $\Sigma\Delta$ modulator in software from which the ternary stream is generated. The simulations are repeated for different amplitudes of the ideal analog sinusoid, in order to cover the whole input dynamic range.

Figure 14 plots the SNDR versus the amplitude of the ideal analog sinusoid which is also the amplitude of the sinusoid encoded in the ternary stream and bitstream. The ternary stream and bitstream allow us to estimate correctly the SNDR until an input amplitude of −12 dBFS. With the bitstream we begin to underestimate significantly the SNDR at −8 dBFS. In contrast, with the ternary stream, we estimate SNDR with a maximum difference of 3 dB until −4.5 dBFS at which point the $\Sigma\Delta$ modulator starts overloading even for the ideal analog sinusoidal stimulus.

5.3 Nominal and Extreme Variations

According to the simulation guidelines in Sect. 4, first, the $\Sigma\Delta$ modulator is divided into sub-blocks and, for these sub-blocks we extract the behavioral parameters that capture the pertinent information. Then, we run $n = 10^3$ transistor-level Monte Carlo simulations of each sub-block using the same seed to obtain n vectors of behavioral parameters. A Monte Carlo analysis samples by definition the statistically likely cases. To examine the accuracy of the proposed built-in test technique across the feasible space of parameters, we perform a LHS of size $n' = 10^3$ in the space of behavioral parameters defined by minimum and maximum values that are fixed at 6σ based on the initial Monte Carlo sample [14]. This synthetic set of behavioral parameter vectors span beyond the most likely feasible space to emulate instances that exhibit extreme variations.

5.4 Parametric Test Metrics Estimation

Behavioral simulations were carried out for each of the $n + n'$ behavioral parameter vectors considering three different test stimuli: an ideal analog sinusoid with amplitude −4.5 dBFS which corresponds to the highest SNDR in Fig. 14,

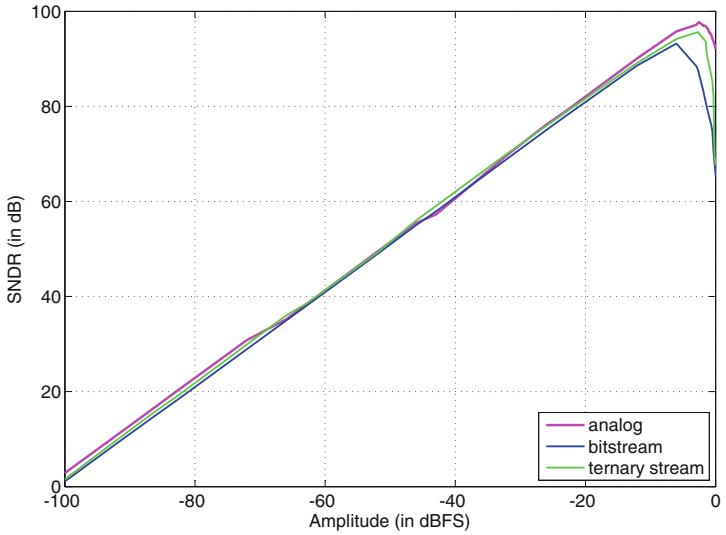

Fig. 14. SNDR across the dynamic range obtained with the standard analog test and by using the bitstream and ternary stream as test stimuli.

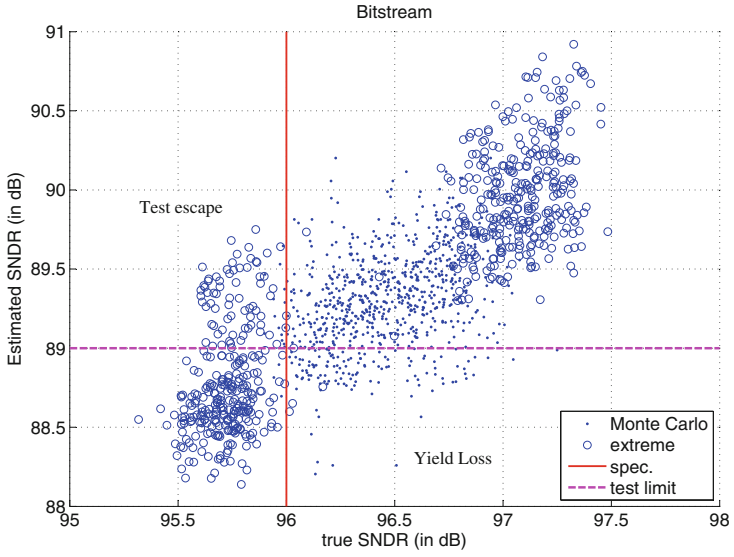

Fig. 15. SNDR estimates obtained by applying the bitstream compared to the true SNDR values obtained by applying the standard analog test stimulus.

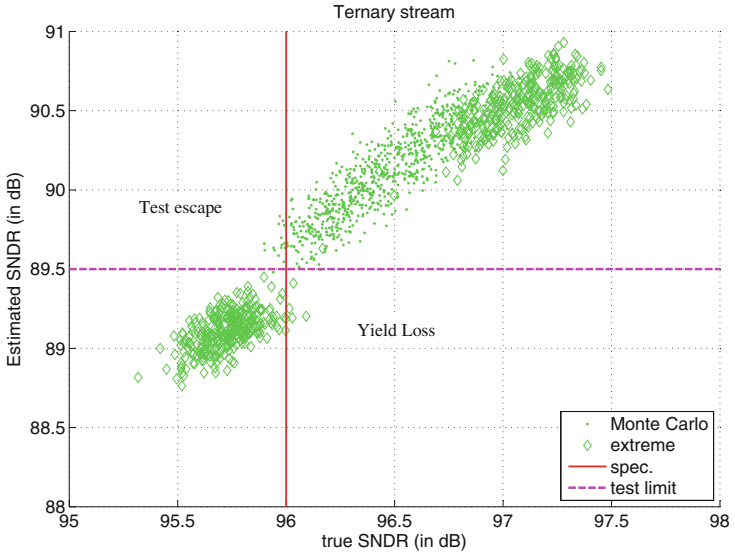

Fig. 16. SNDR estimates obtained by applying the ternary stream compared to the true SNDR values obtained by applying the standard analog test stimulus.

an optimized ternary stream where an ideal analog sinusoid with amplitude −12 dBFS serves as the input to the ideal $\Sigma\Delta$ modulator in software, and the selected bitstream from the output of the ideal $\Sigma\Delta$ modulator in software from which the ternary stream is generated.

Figure 15 projects the $n + n^{'}$ instances onto the space defined by the true SNDR obtained by applying the ideal analog sinusoidal stimulus and the estimated SNDR obtained by applying the bitstream. Similarly, Fig. 16 shows the same result for the ternary stream. The solid points in Figs. 15 and 16 correspond to the n Monte Carlo instances while the circles in Fig. 15 and the diamonds in Fig. 16 correspond to the $n^{'}$ samples derived by LHS. The Monte Carlo instances are distributed around the nominal point while the extreme samples derived by LHS are distributed away from the nominal point at the upper right and lower left corners of the scatter plot. The SNDR specification of the $\Sigma\Delta$ modulator under test is fixed at 96 dB and it is shown in Figs. 15 and 16 with a vertical line. As it can be seen, most of the n Monte Carlo instances lie on the right side of the line, i.e. they satisfy the specification. Looking at the distribution of instances along the y-axis, we observe from Figs. 15 and 16 that the SNDR obtained by applying the bitstream presents a much larger variation and has a lower mean value compared to the case of the ternary stream. This is explained by the fact that the bitstream overloads the $\Sigma\Delta$ modulator under test to a larger degree compared to the case of the ternary stream. It can also be seen that the ternary stream results in SNDR estimates that correlate well with the true SNDR while for the bitstream the correlation is less apparent.

Test limits on the estimated SNDR can be placed to achieve the best trade-off between parametric test escape and yield loss. A possible selection of test limits is shown in Figs. 15 and 16 with the horizontal lines. Since the ternary stream leads to a better correlation between the true and estimated SNDR as opposed to the bitstream, we observe that the test escape and yield loss is much lower. Regarding the bitstream, any placement of the test limit will result inadvertently to test escape and/or yield loss.

6 Conclusion

In this chapter, we described a BIST technique for the SNDR performance of $\Sigma\Delta$ ADCs together with an advanced simulation framework for its thorough validation. The BIST technique is nearly fully digital with minimal modifications in the analog part of the ADC. It relies on the injection of a ternary stream test stimulus at the input of the ADC. It is shown that a ternary stream is more efficient than a bitstream in terms of stimulus dynamic range, as well as in terms of the resultant parametric test metrics, such as test escape and yield loss. Moreover, the actual values of the SNDR and the estimates obtained by applying a ternary stream correlate very well, which makes the proposed BIST practically equivalent to the standard test using a high-resolution analog sinusoid supplied from the ATE.

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