8T-SRAM Cell with Improved Read and Write Margins in 65 nm CMOS Technology

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Abstract. SRAM operation at subthreshold/weak inversion region provides a significant power reduction for digital circuits. SRAM arrays which contribute to a large amount of power consumption for the processors in sub-100 nm technologies, however, cannot benefit from subthreshold operation. To this end, new SRAM technique on the circuit or architecture level is required. In this chapter, a novel 8T-SRAM cell is proposed which shows a significant improvement in write margin by at least 22 % in comparison to the standard 6T-SRAM cell at supply voltage of 1 V. Furthermore, read static noise margin of the proposed cell is improved by at least 2.2X compared to the standard 6T-SRAM cell. Although by the use of the proposed SRAM cell, the total leakage power is increased for superthreshold region, the proposed cell is able to work at supply voltages lower than 200 mV through which the total power consumption and the robustness of the cell are improved significantly. The proposed circuit is designed in 65 nm CMOS TSMC technology.

Keywords: SRAM · Subthreshold · Low-power · Write margin

1 Introduction

SRAM memories take up to 80 % of the total die area and up to 70 % of the total power consumption of high-performance processors [1]. Therefore, there is a crucial need for high-performance, low-leakage, and highly robust SRAMs. Unfortunately by scaling the CMOS technology, particularly under scaled supply voltages, both read and write stabilities are affected by the existing intra- and inter-die variations. Furthermore, due to the use of large number of small geometry transistors in a memory array, process variations have a significant impact—leading to possible read, write, and hold failures. Furthermore, in standard 6T SRAMs, the conflict between read and write stabilities is an inevitable design constraint that needs to be considered meaning that by improving the write margin, read margin is degraded and vice versa.

To improve the SRAM cell functionality, several solutions have been proposed from device to architecture level. For instance, the use of new devices such as FinFETs that leads to a significant performance improvement [2–5]. At the cell level, new cells such as 7T, 8T, 9T, 10T, and 11T [6–15] have been proposed with the focus on improving read static noise margin (RSNM) or write margin (WM). At the architecture

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level, proposed read and write assist techniques in literature can improve SRAM robustness and performance while occupying less area compared to the cell techniques (e.g. 8T and 10T) and can be used with any type of SRAM [16, 17]. To understand the existing challenges in SRAM design let us explain the operation of standard 6T-SRAM cell.

The standard 6T-SRAM cell is shown in Fig. 1 that consists of two back-to-back inverters (includes two pull-up PMOS and two pull-down NMOS transistors) and two NMOS access transistors connected to the bitlines with the gates connected to the wordline. During read, wordline is asserted and the voltage difference between bitlines is sensed using a sense amplifier. The read cycle is done via access transistors and the pull-down transistors. Stronger pull-down transistors (PDL and PDR) and weaker access transistors improves RSNM. On the other side, stronger access transistors and weaker pull-up transistors improves WM. Through upsizing, the SRAM cell can operate at very low supply voltages (i.e. low VDD_{min}) with minimized threshold voltage variation with a penalty of increased area. However, continuously increasing process variations in sub-100 nm technologies has led to a pronounced degradation in stability of SRAM cells especially at lower voltages.

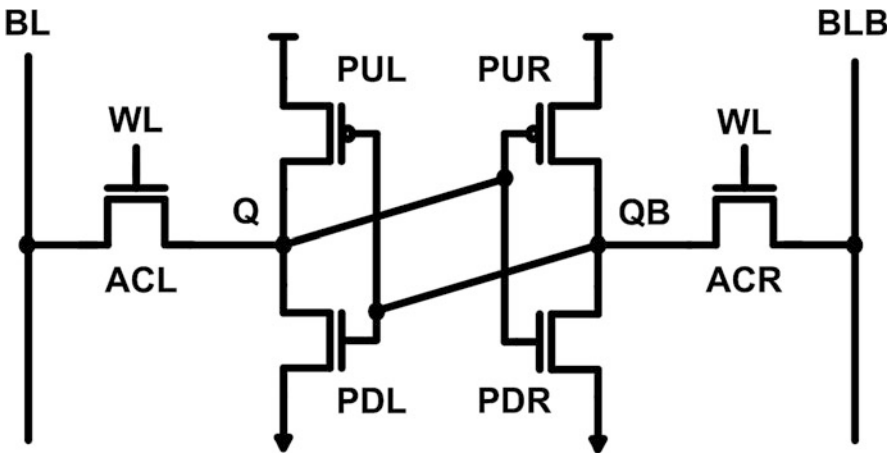

Fig. 1. 6T-SRAM cell using CMOS technology.

To overcome this issue, different cell techniques such as 8T-SRAM cell ameliorates the degraded robustness of the standard 6T-SRAM cell by separating read and write bitlines leading to a significant improvement in read static noise margin (RSNM) while the write margin is not affected. The standard 8T-SRAM cell is shown in Fig. 2. As it is seen, read and write cycles use different wordlines and bitlines. Noted, the standard 8T-SRAM cell uses a single-ended read scheme which reduces the swing of bitlines. The 8T-SRAM cell provides significantly improved RSNM (similar to the Hold Static Noise Margin (HSNM) of the standard 6T-SRAM cell) with similar access time, write time, and write margin. However, for the 8T-SRAM cell write assist techniques such as boosted wordline without affecting the read performance can be used.

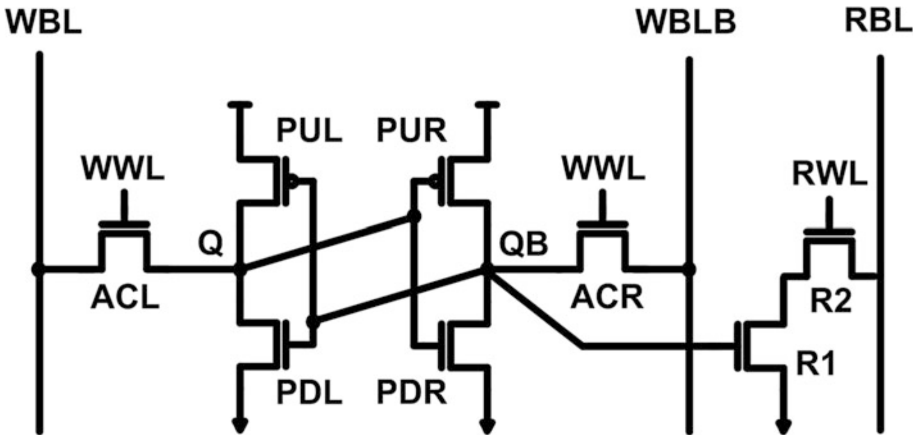

Fig. 2. Standard 8T-SRAM cell [13].

Therefore, proposing a new SRAM cell to improve both read and write margins under scaled supply voltages is crucial for ultra-low power applications with low penalty on area, access time, and leakage power consumption.

In this chapter, a novel 8T-SRAM cell is presented that improves both read and write operation margins. The proposed SRAM cell improves write and read noise margin by at least 22 % and 2.2X compared to the standard 6T-SRAM cell, respectively. Furthermore, this method reduces gate leakage while increases subthreshold leakage compared to the standard 6T-SRAM cell in 65 nm CMOS technology. In general, leakage power of the proposed cell increases by 67 % at V_{DD} = 1 V and 5.6 % at V_{DD} = 300 mV. The proposed design improves the leakage power by 3 % at V_{DD} = 200 mV. The threshold voltage of the transistors used in this paper is 300 mV.

The rest of this chapter is structured as follows: in Sect. 2, the new 8T-SRAM cell is presented and described in different modes of operation. In Sect. 3, the simulations results are presented and discussed. We conclude in Sect. 4.

2 The Proposed 8T-SRAM Cell

Figure 3 shows the proposed 8T-SRAM cell where two transistors, one NMOS and one PMOS are added to the standard 6T-SRAM cell while the mechanism of read is single-ended [18]. During read, only RWL is asserted while during write both WWL and RWL signals are set to high. In this SRAM cell structure, transistor PUC is used to improve the write margin of the circuit when a “1” is stored on the storage node Q. In this mode, when the value on QB is “0”, the voltage on the drain of NF increases that weakens the drivability of PUC. Therefore, writing “0” on storage node becomes easier. When QB keeps “1”, however, the write margin is not expected to be improved. In this case, to improve the write margin of SRAM cell, PUR is sized smaller than PUL that results in an improved write margin in this mode as well. During read, ACL turns on while ACR is kept in cut-off region. When Q holds a “0”, transistors PDL and NF

help to discharge the bitline capacitance to a level to be sensed by a sense amplifier. In this mode, transistors PDR, PUL, and ACR are OFF. Sizing down the transistor PDR will improve read margin due to the fact that the discharging path of QB to ground is weakened. Noted, the stacking effect lowers the current through the transistor PDR. In case the node Q holds a “1”, transistor NF is OFF. Therefore, no discharging path exist from node Q to ground that results in significant improvement in read static noise margin (RSNM). In general, RSNM of the proposed circuit is improved by at least 2.2X compared to the standard 6T-SRAM cell and is similar to the standard 8T-SRAM cell considering this fact that write margin is not improved in the standard 8T-SRAM cell. During hold, both RWL and WWL signals are set to low turning off the access transistors. The data retention of this cell depends on the bit stored on the cell. When Q holds a “1” the node QB will be floating that will give an uncertainty of the circuit. Although, the level of voltage on node QB is not zero, due to the stacking effect of PDR-NF where the drain of the transistor NF goes to a level equals to the voltage on node QB, the transistor PDR will turn off completely. However, when storage node is holding a “0”, the data retention improved due to the fact that both NF and PDR are ON that keeps “0” at node QB.

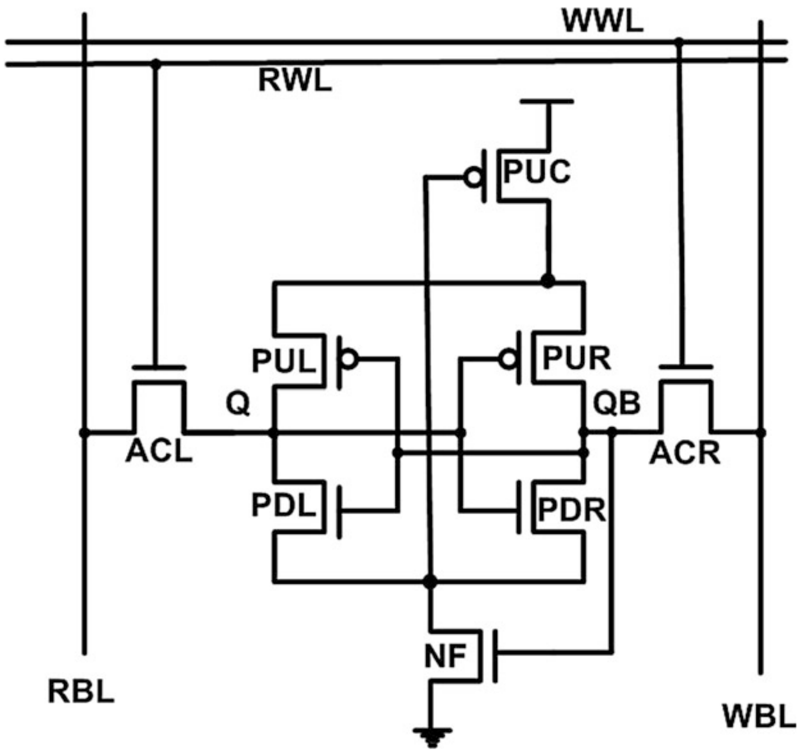

Fig. 3. Proposed 8T-SRAM cell.

Similar to the standard 8T-SRAM cell, the proposed cell uses a single-ended read approach which definitely reduces the swing of the output. However, different techniques can be used to compensate this effect such as a pseudo-differential sensing scheme that can be used for our proposed SRAM cell [19].

The simulation results for the circuit for different modes will be discussed in the next section.

3 Simulation Results and Comparison

Simulation results are done using 65 nm CMOS technology models at room temperature (i.e. 27° C) at different supply voltages from subthreshold to superthreshold to region. In this section, the proposed SRAM cell is simulated at different modes of operation.

To evaluate the read stability of an SRAM cell Read Static Noise Margin (RSNM) is used. RSNM is defined as the length of the side of the largest square that can fit into the lobes of the butterfly curve. Butterfly curve is obtained by drawing and mirroring the inverter characteristics while access transistors are ON and bitlines are precharged to V_{DD} [20]. For the proposed SRAM cell, however, only left side of the circuit defines the stability of the circuit. The reason is attributed to this fact that, when Q holds "1", increasing the value of QB even to very large values does not change the data stored on node Q. To this end, we simulate the proposed SRAM cell for cases Q = "0", WWL = "1", and RWL = "0" (i.e. CASE 1) and also Q = "1", WWL = "1", and RWL = "0" (i.e. CASE 2). The shadowed part of Fig. 4 shows the operation of the proposed SRAM cell when WWL is asserted and RWL signal is low. Here, we consider two cases. In CASE 1, node QB discharges via transistor ACR to ground that is a successful write while RWL is kept at "0". However, in CASE 2 where Q holds "1", although the voltage on node QB increases to 0.4 V, the value on node Q is not flipped. This proves a very high robustness of circuit even at very high input noises when Q stores "1". This concludes that single ended writing will fail (i.e. CASE 2) that leads us to turn on both access transistors during write cycle. The results for RSNM of the proposed SRAM cell compared to the standard 6T-SRAM cell at different supply voltages are shown in Fig. 5. As it is shown, 2.66 X improvements in RSNM is achieved by the use of the proposed 8T-SRAM cell compared to the standard 6T-SRAM cell. At lower supply voltages such as 200 mV, the proposed 8T-SRAM cell shows 4.86X improved RSNM. Due to this fact, the proposed SRAM cell is able to operate with a high margin at very low supply voltages (i.e. subthreshold/weak inversion region). However, the standard 8T-SRAM cell shows slightly better RSNM compared to the proposed 8T-SRAM cell.

To clarify the operation of the proposed circuit, the SRAM operation at different modes is shown in Fig. 6. As it is shown, during read, when Q holds "0", while the BL has been discharged to 300 mV, voltage on node Q is not increased higher than 0.2 V that is due to the stacking effect of transistors from node QB to ground and the small size of the transistor PDR in the cell (Fig. 6(b)). This confirms the robustness of the proposed circuit during read (i.e. RSNM). The successful writing "0" is shown in Fig. 6(a) when both RWL and WWL are set to high.

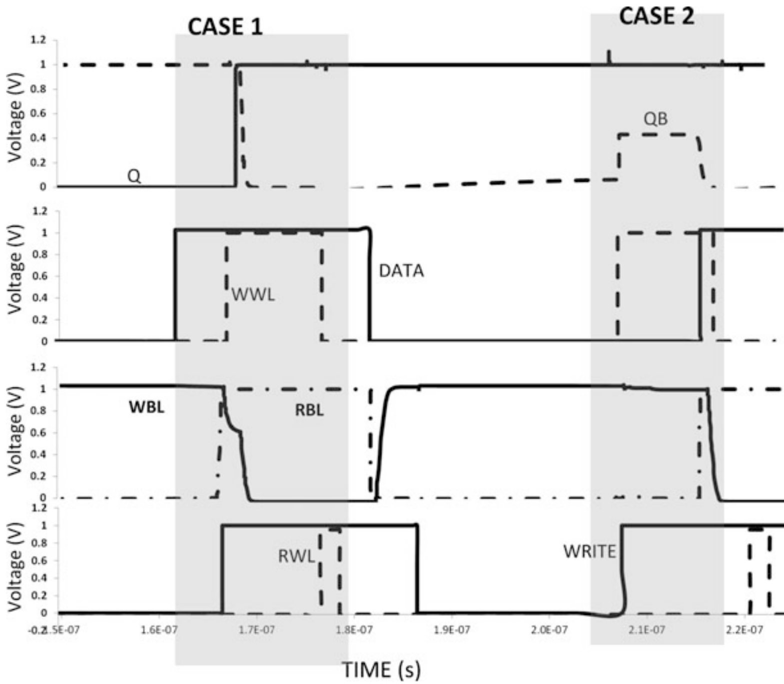

Fig. 4. Waveforms of the proposed 8T-SRAM cell (Shadowed part shows when WWL = "1" and QB = 1 or "0").

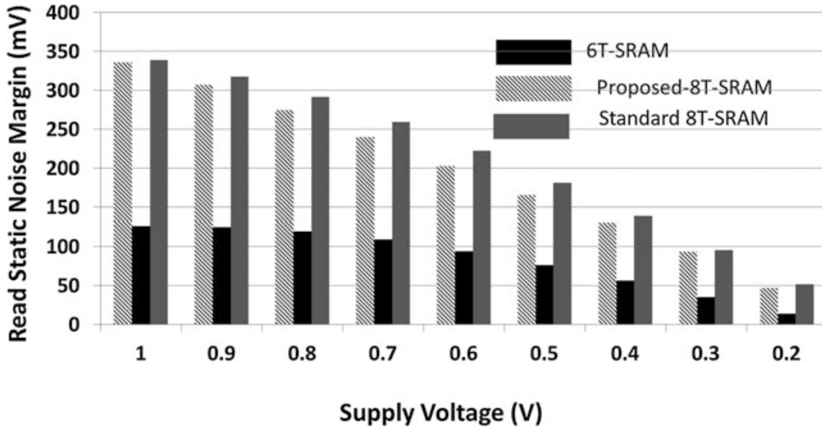

Fig. 5. RSNM results for the standard 6T-SRAM, 8T-SRAM and the proposed 8T-SRAM cell.

Write margin is another metric used to evaluate the stability of an SRAM cell in write mode. Different methods have been used to find the WM of an SRAM cell [21]. For the WM simulations, we choose the Word-Line (WL) voltage sweep method. In this method the bitline will be connected to the appropriate voltages to enable flipping

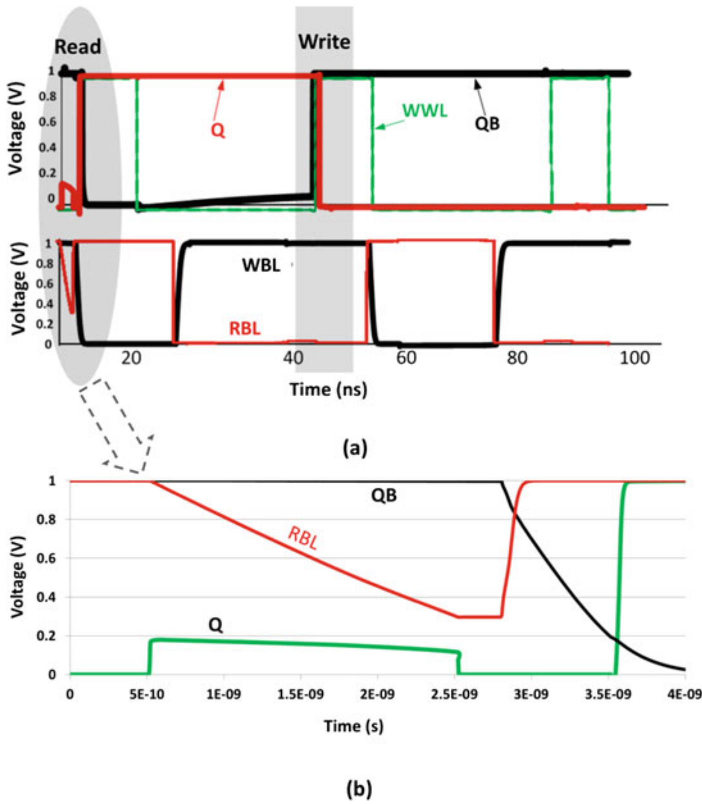

Fig. 6. (a) The proposed 8T-SRAM cell waveforms (b) read operation.

the data on the storage node. Then WL and WLB are swept from 0 V to 1 V and 1 V to 0 V, respectively. WM is calculated as the difference between V_{DD} and WL voltage when the data stored in the cell is flipped. Figure 7 illustrates the write margin of the proposed 8T-SRAM cell versus the standard 6T-SRAM cell. As it can be seen, when writing "0", the proposed 8T-SRAM improves the write margin between 28 %–73 % at different supply voltages. The proposed 8T-SRAM cell improves write margin by at least 21 % when writing "1". As it is shown in Fig. 7, improvement in write margin of the proposed circuit is increased at lower supply voltages enabling this circuit to work at extremely low supply voltages. Figure 8 shows an example of writing "0".

To achieve improvements in both read and write, the proposed 8T-SRAM cell must be sized carefully. To achieve the best write improvement when writing "1", PUR is sized smaller than PUL. In addition, improved read noise margin can be achieved by down-sizing the PDR transistor. The sizing of the proposed 8T-SRAM cell used is tabulated in Table 1.

Another important metric for An SRAM cell is leakage power consumption. To measure the leakage power consumption of the proposed SRAM cell compared to the standard 6T-SRAM cell, the leakage current of each transistor was measured that is

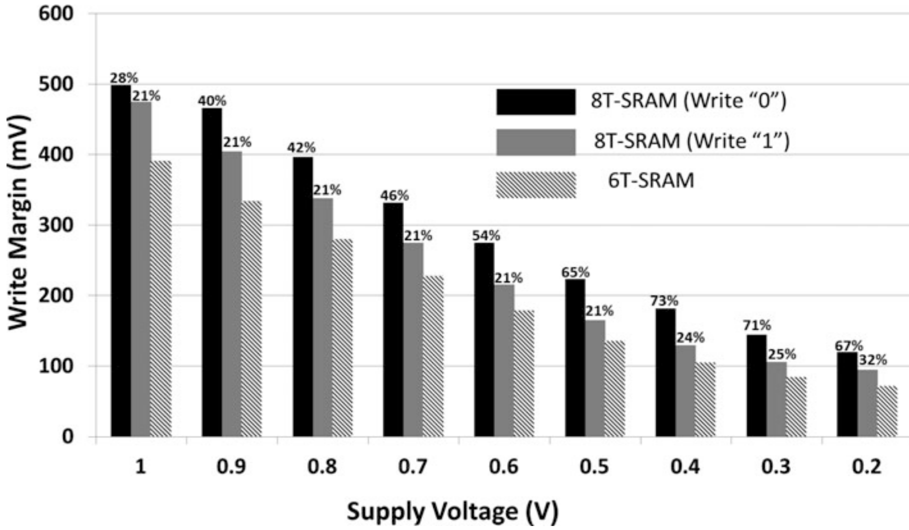

Fig. 7. Write margin of the proposed 8T-SRAM cell versus the standard 6T-SRAM cell when writing "0" and "1" (the standard 8T-SRAM provide negligibly smaller WM in comparison to the standard 6T-SRAM cell).

shown in Table 2. As it is shown the leakage through access transistors is reduced significantly that is attributed to the raised voltage level of storage node holding "0". However, the total leakage current of the proposed cell is increased when the stored bit is "1" while in case of Q = "0", the total leakage of the proposed cell is less than the standard 6T and 8T-SRAM cells. For this simulation a bitline capacitance of 200fF and the supply voltage of V_{DD} equals to 1 V at room temperature have been considered. To show the power degradation of the proposed SRAM cell at different supply voltage, we calculate the total power consumption of the proposed cell versus the standard 6T-SRAM and 8T-SRAM cells for V_{DD} = 1 V to V_{DD} = 200 mV. As it is shown in Fig. 9, leakage power of the proposed SRAM cell compared to the standard 6T-SRAM cell is degraded by 14.2 % and 67 % for supply voltages of 0.2 V and 1 V, respectively when the stored bit is "0" while for the case of Q="1", the proposed cell improves the leakage power by 34 % and 23 % at supply voltage of 1 V and 0.4 V, respectively. In comparison to the standard 8T-SRAM cell for the case of Q = "1", leakage current is degraded by 7 % to 21 % for VDD = 0.2 V and 1 V, respectively while for the case of Q = "0", the leakage current of the proposed cell increases by 20 % and 43 % for VDD = 0.2 V and 1 V, respectively.

In this part, the access time and the write time of the proposed circuit is explored in comparison with the standard 6T and 8T-SRAM cells [6]. Access time is measured as the time required for discharging the bitline voltage so that the difference between bitline voltage and V_{DD} (i.e. V_{sense}) can be sensed by the sense amplifier circuit. To this end, we simulate the proposed 8T-SRAM cell at supply voltage of V_{DD} = 300 mV at room temperature. Figure 10 illustrates the comparison between the proposed 8T-SRAM cell versus standard 6T-SRAM and the 8T-SRAM cells. As it is seen, the

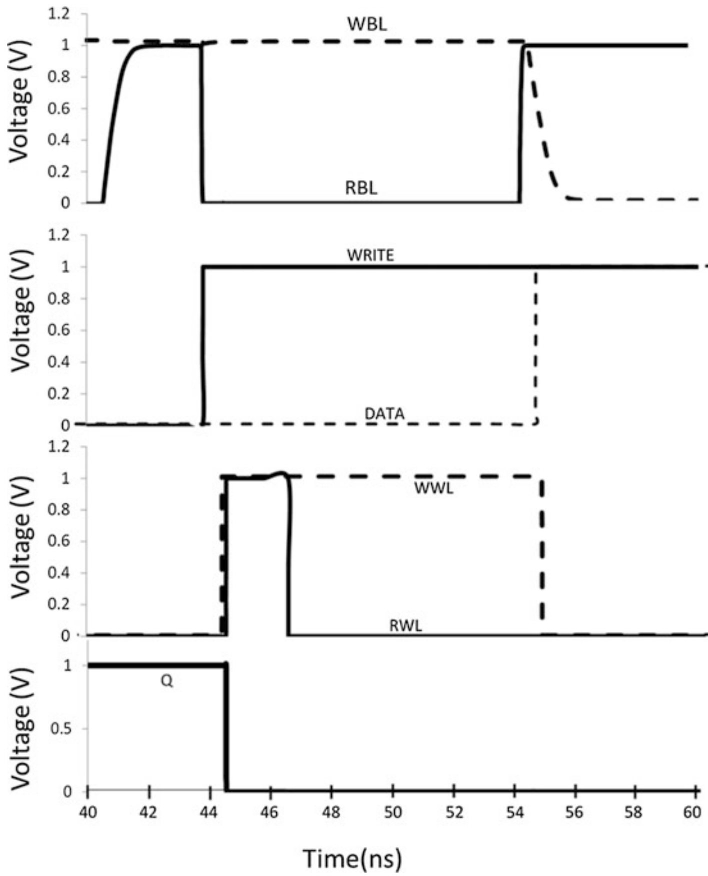

Fig. 8. Write "0" for the proposed 8T-SRAM cell.

Table 1. Sizing of the standard 6T, 8T and the proposed 8T-SRAM cells.

6T-SRAM cell		Proposed 8T-SRAM		Standard 8T-SRAM	
ACL, ACR	180n	ACL, ACR	180n	ACL, ACR	180n
PDR	230n	PDR	200n	PDR,PDL	200n
PUL	230n	PUL	150n	PUL	150n
PUR, PDR	150n	PUR	120n	PUR	150n
		PUC	150n	R1	180n
		PDL, NF	300n	R2	230n

maximum degradation is at lower supply voltage due to the weakened drivability of the transistors at lower supply voltages. The maximum degradation is at 200 mV (21 %) which improved by increasing the supply voltage. For instance, at V_{DD} = 600 mV, the access time degradation is only 4 % compared to the standard 6T and 8T-SRAM cells and all the circuit show similar access time at V_{DD} = 800 mV and above.

Table 2. The leakage current of the standard 6T and the proposed 8T SRAM cells.

6T-SRAM Current (nA). G:gate, D: Drain, and S: Source				Proposed 8T-SRAM Current (nA). G:gate, D: Drain, and S: Source				Standard 8T-SRAM Current (nA). G:gate, D: Drain, and S: Source			
Tr.	*G*	D	S	Tr.	G	D	S	Tr	G	D	S
ACL	0.323	0.017	0.15	ACL	0.36	0.084	0.209	ACL	0.1	1.3	1.16
ACR	*0.153*	1.802	1.853	ACR	0.144	0.178	0.187	ACR	0.23	0.098	0.104
PUL	0.563	4.191	4.767	PUL	0.462	2.95	3.428	PUL	0.115	1.13	1.01
PUR	0.208	1.856	1.66	PUR	0.122	1.132	0.979	PUR	0.31	2.69	2.68
PDL	0.234	2.361	2.103	PDL	0.246	1.497	1.73	PDL	0.52	2.72	3.24
PDR	1.47	4.455	5.892	PDR	0.887	3	2.02	PDR	0.114	1.37	1.24
				PUC	0.47	4.42	4.896	R1	1.10	3.90	1.13
				NF	0.001	4.967	5.025	R2	0.57	1.02	0.075

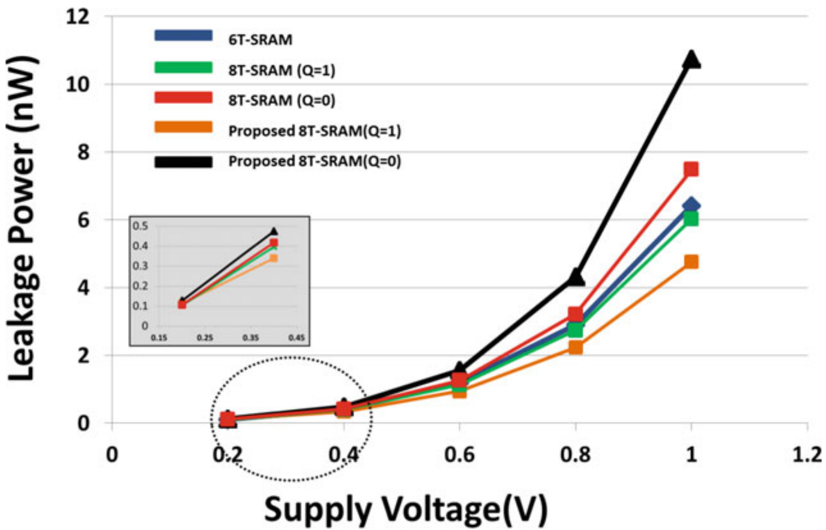

Fig. 9. Leakage power increase percentage for proposed 8T-SRAM cell versus the standard 6T-SRAM cell.

Another metric to compare different SRAM topologies is write time. In the proposed circuit due to the increased write margin, it is expected a faster data flipping on storage nodes during write cycle. Due to the asymmetry nature of the proposed SRAM cell, we simulate the cell for write "0" and write "1". Figure 11(a) and (b) illustrate the proposed SRAM cell behavior for both cases. As it is seen, the proposed SRAM cell provides faster write during write "0" compared to write "1" that is attributed to the weakened pull-up path through which the contention between PMOSs and access transistors is reduced. Figure 12 shows a comparison between the proposed SRAM cell versus the standard 6T and 8T SRAM cells at supply voltage of 600 mV. Here, the write time improvement percentages provided by the proposed cell over the standard

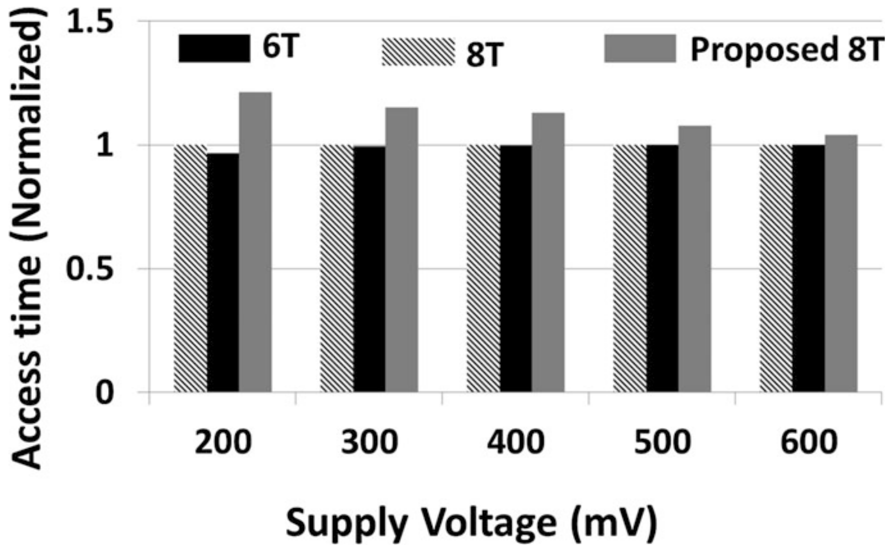

Fig. 10. Access time comparison for different SRAM cells (access time is normalized to the access time of the standard 6T-SRAM cell at different supply voltages).

6T and 8T SRAM cells during write “0” and write “1” are 25 % and 12 %, respectively. Noted, the improvement for write time at lower supply voltages is degraded due to the weakened driving current of transistors in the stacked configuration of the proposed SRAM cell. To this end, the use of low-Vth transistors can help to solve the low drivability of the stacked transistors with the penalty of area overhead.

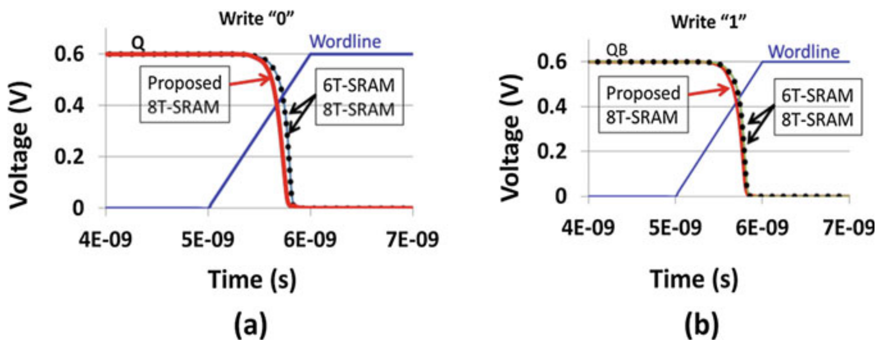

Fig. 11. (a) Write “0” and (b) write “1” for the proposed 8T-SRAM cell at V_{DD} = 0.6 V.

One of the main issues for the proposed 8T-SRAM cell is floating storage node (QB) when the stored data is “1”. Therefore, a thorough discussion for the proposed cell is required to evaluate the cell operation. As mentioned, during hold, read “1”, and write “1”, the storage node QB is grounded which turns off the NF transistor disconnecting the floating node from ground. Therefore, the proposed circuit is simulated

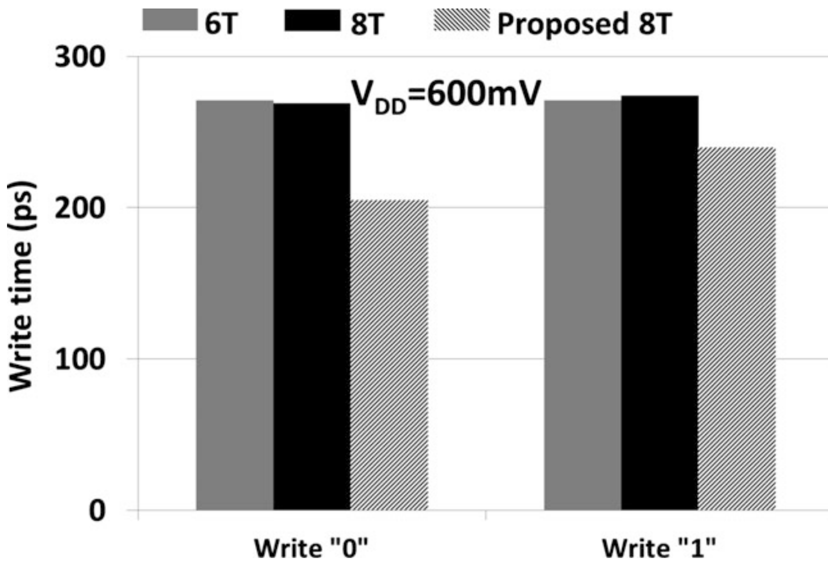

Fig. 12. Write time comparison between the standard 6T and 8T SRAM cells with the proposed 8T-SRAM cell.

for each cycle. During hold, the drain of NF is charged to a voltage equals to 53.5 mV which is equals to the voltage on node QB. The circuit was simulated for a long stay in hold time which shows the voltage on nodes QB and the drain of NF becomes equal and fixed at 53.5 mV. This leads to a turned-off transistor PDR which reduces the leakage current through storage node to ground. All three SRAM cells were simulated to measure their leakage current through storage nodes to ground under same condition.

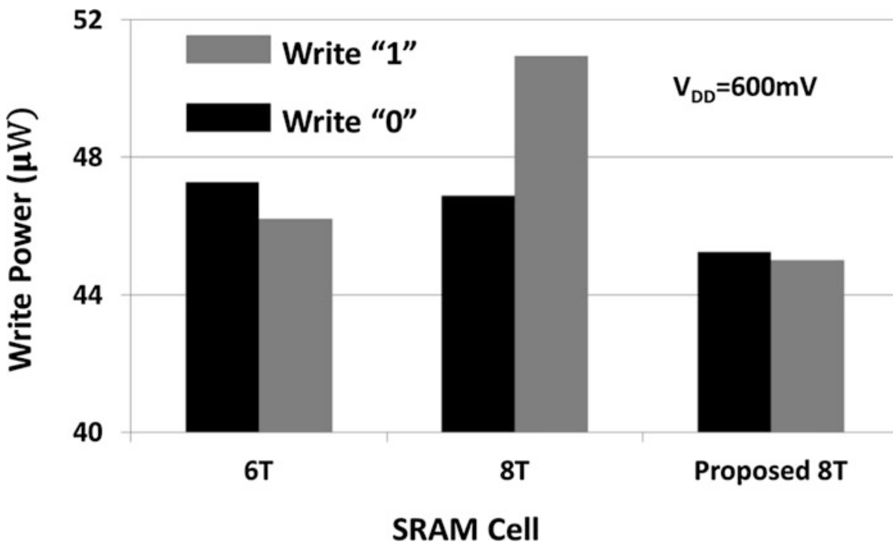

Fig. 13. Write power consumption for different SRAM cells.

During hold, we measured the leakage through transistors connected to ground to get an estimation of the total leakage when the node QB is floating. Simulation results show a fixed leakage current of 1.72 nA through pull-down transistors to ground while the standard 6T and 8T SRAM cells show a total leakage current of 2.59 nA and 2.63 nA through transistors connected to ground, respectively. However, as shown before, the total leakage power of the proposed circuit is higher than as for the standard 6T-SRAM cell when the stored data is "0".

During write "0", as explained in Sect. 2, the QB node is floating which helps to improve the write margin and write time. Based on this fact, the total write power is reduced, as well. To this end, the total power consumption of the standard 6T and 8T is compared with the proposed 8T-SRAM cell which is shown in Fig. 13. As it is seen, the proposed design provides minimum write power consumption during write "0" which is attributed to the floating node QB and drain of transistor NF.

During read due to the single-ended structure of the proposed circuit in which the node QB is decoupled from bitline, it will not affect the read process. Assuming that the

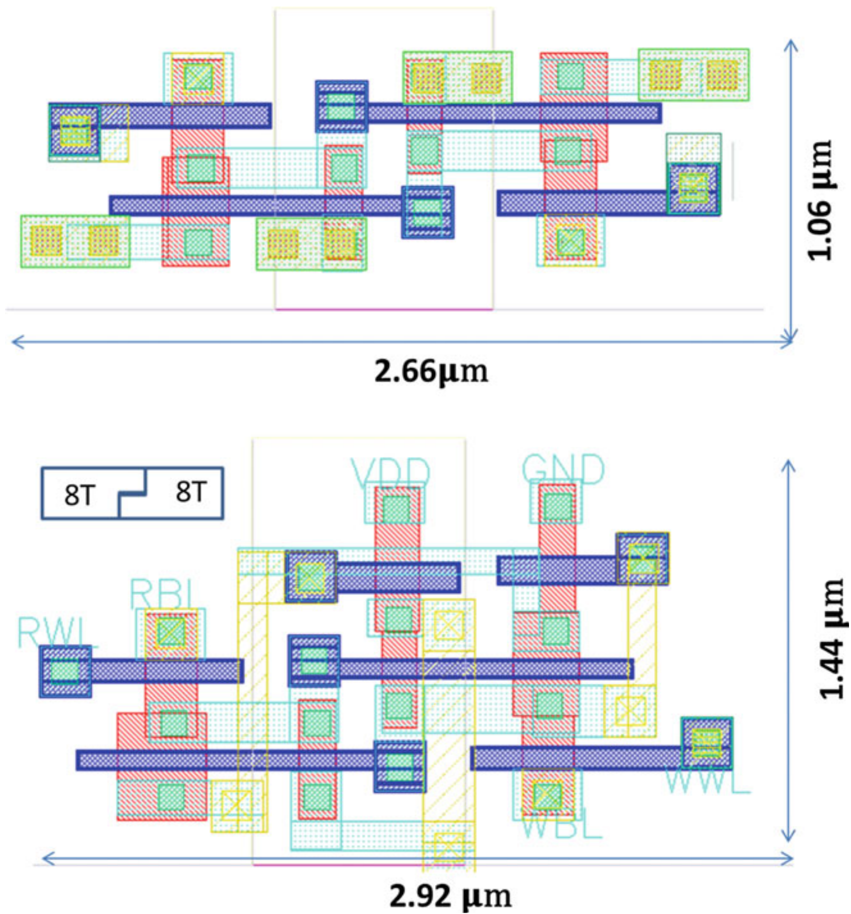

Fig. 14. Write power consumption for different SRAM cells.

voltage on node QB is 53.5 mV, it will continue to keep this voltage during read, as well. To evaluate the cells during read “1”, the read power consumption of each circuit was measured. The standard 6T and 8T SRAM cells consume a read power of 119.46 nW and 1.9758 nW, respectively, while the proposed 8T-SRAM consumes 0.93 nW (930 pW). Consequently, we can claim that the floating node QB has no effect on the performance as well as it improves the power consumption during read and write.

Finally, the area of the proposed circuit in comparison to the standard 6T-SRAM cell is shown for a single cell. As it is shown in Fig. 14, the proposed technique increases the area by 49 % in comparison the standard 6T-SRAM cell. However, due to the L-shape of the cell layout, the total area overhead of the cell will be reduced. The standard 8T-SRAM cell, however, introduces 33 % area overhead in TSMC 65 nm technology.

All in all, the proposed SRAM cell, similar to the standard 8T-SRAM cell, improves read margin significantly while the write margin is improved, as well. Therefore, the proposed design has the advantages of improved write margin and write-time over the standard 6T and 8T-SRAM cells. Due to the asymmetric nature of the proposed SRAM cell, write margin improvement when writing “0” is larger than the case of “1”. Therefore, as mentioned, by careful sizing of the transistors in our design, higher write margin (i.e. more symmetric write) will be achieved that enables designers to scale the supply voltage aggressively for ultra-low power applications.

4 Conclusions

In this chapter, a new 8T-SRAM cell was discussed which shows improvement in read and write margins by 2.2X and 22 %, respectively, compared to the standard 6T-SRAM cell. In addition, the proposed design improves the gate leakage power consumption while increases the subthreshold leakage compared to the 6T-SRAM cell. All in all, the proposed design improves read and write margins without any penalty in leakage power at subthreshold region compared to the standard 6T-SRAM cell. Furthermore, the proposed 8T-SRAM cell has a superior advantage of improved write margin in comparison to the standard 8T-SRAM cell.

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