Chapter 16
EMC Design Guidelines

Everything should be made as simple as possible, but no simpler.

—Albert Einstein

16.1 Most Common EMC Issues in Practice

The guidelines in this chapter are biased by the author's own experience, gathered during many years of electronics development, firmware programming, and systems engineering. This should be mentioned here as a kind of a disclaimer and that you, the reader, can better understand how to weigh and classify the guidelines presented here.

From the author's own experience, these are the most common EMC issues during product development:

- **Radiated emissions.** Many products regularly fail radiated emissions EMC testing from 30 MHz to 6 GHz according to CISPR 32 or CISPR 11. Most issues typically occur in the frequency range <1 GHz, where the causes of radiation are usually cables or units within the system which are not grounded properly. If the emission limits for $f > 1$ GHz cannot be met, the unintentional radiator can most probably be found on a PCB (clock lines, single-ended high-speed data lines, small PCB-structures).
- **Radiated immunity.** Radiated immunity for most products requires testing according to IEC 61000-4-3. Usually, sensors are the most sensitive elements in a product. This is why sensors require special attention during the design and EMC immunity testing. Care must be taken that all signal lines to and from a sensor are filtered with the maximum allowed attenuation. However, every filter causes distortions and time delays (phase shift in the frequency-domain). Therefore, ensure that the distortions and time delays are below the allowed maximum. In addition, low-impedance grounding of any sensitive circuit is of utmost importance and the cabling and PCB-structures should be kept as short and small as possible.

R. B. Keller, *Design for Electromagnetic Compatibility–In a Nutshell*,
https://doi.org/10.1007/978-3-031-14186-7_16

- **Electrostatic discharge.** Grounding, grounding, grounding. ESD testing is performed according to IEC 61000-4-2. Every electrically floating part of a product increases the chance of failing the ESD-test because it increases the chance that undesired currents—caused by ESD-pulses—flow along wires and PCB signal lines and eventually lead to damaged integrated circuits or disturbed signals.

16.2 Guideline # 1: Never Route Signals Over Split Reference Planes

Goal = reduced radiated emissions.
Do not route signals over split return signal reference planes (GND, power planes)! Never! This leads to unnecessary large current loops (as the current return cannot flow directly underneath the forward current, Fig. 16.1) and large current loops tend to lead to high radiated emission values.
Rule of thumb: Whenever in doubt, do not split return current reference planes (GND, power planes). Go with a solid-filled reference plane instead. There must be a good reason for splitting planes! There should always be at least one solid reference plane closely adjacent to high-frequency signals ($f > 1$ MHz).

16.3 Guideline # 2: Always Consider the Return Current

Goal = reduced radiated emissions and common-impedance coupling.
Always consider the return current! Always! And with the return current in mind, minimize the common return current paths of high-current circuits (e.g., motors) and sensitive circuits (e.g., unamplified sensor signals) because these common paths lead to common-impedance coupling (see Sect. 12.1.1). In addition, try to minimize the loop area A [m^2] between the forward and return current of high-frequency signals because these loops may lead to unintended radiated emissions (see Sect. 9.9.1).
Hint: Assuming a high-frequency signal s_1 ($f > 1$ MHz) along a PCB trace on layer 1 and a reference plane (e.g., GND or power plane) on layer 2, the return current of the high-frequency signal s_1 on the reference plane prefers to flow directly under the trace of s_1 because the high-frequency return current always takes the path of the least inductance (see Sect. 14.4).

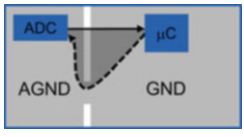

Fig. 16.1 Signal and its return current path in case of split ground planes

16.4 Guideline # 3: Decoupling—Use Low-Inductance Capacitors AND Planes

Goal = reduced radiated emissions and common-impedance coupling.
Decoupling is important! (Fig. 16.2) Always consider decoupling!
Hint: Decoupling depends on the number of PCB layers and stackup:

- **Two- and single-layer PCBs.** For single- or two-layer PCB designs, place the decoupling capacitors as close as possible to every power supply pin of every chip of the PCB. This refers to *local decoupling*.
- **Multi-layer PCBs.** In the case of multi-layer PCB designs with closely spaced GND and power planes (<0.25 mm, <10 mils), the decoupling capacitor location is not as critical as for single- or two-layer designs because the closely spaced planes act as an efficient decoupling capacitor for high-frequencies (>1 MHz) and the actual decoupling capacitor acts as a *global decoupling* capacitance. However, more important than the location of the decoupling capacitor is that the power supply and GND pins of the integrated circuits are connected with low inductance (multiple vias) to the respective planes.

16.5 Guideline # 4: Use Ground Planes on PCB for Shielding

Goal = reduced interference on circuit board.
Use solid-filled reference planes (e.g., GND or power supply planes) on a PCB to separate noise signals (e.g., motor signals) from sensitive signals (e.g., unamplified sensor signals). The reference plane will act as a shield and will lower electromagnetic interference (EMI). However, be aware that such a copper shield will

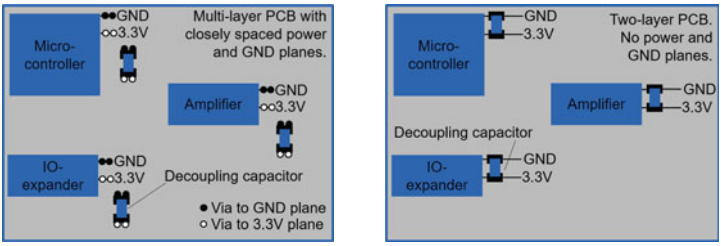

Fig. 16.2 PCB power-supply decoupling. (**a**) PCB with closely spaced power supply and GND planes (global decoupling). (**b**) PCB without closely spaced power supply and GND planes (local decoupling)

primarily be effective for E-fields at any frequency and high-frequency H-fields ($f > 1\,\text{MHz}$), but not for low-frequency H-fields because copper has low relative permeability μ_r' and does not act as a shield against low-frequency magnetic fields.

16.6 Guideline # 5: Route High-Frequency Signals Adjacent to a Plane

Goal = reduced radiated emissions.
High-frequency signals are always to be routed close to an adjacent solid reference plane (GND or power supply plane, which acts in this case as a high-frequency ground). For single-layer designs, use guard traces close to the high-frequency signals where the return currents can flow or GND copper fill.

16.7 Guideline # 6: Control Rise- and Fall-Time

Goal = reduced radiated emissions.
Increase the rise- and fall-time of any digital signal (especially clock signals) as far as possible. A short rise- and fall-time means larger signal bandwidth and, therefore, more high-frequency content in a digital signal, which could lead to radiated emissions or reflections in case of a long transmission line (compared to the wavelength of the high-frequency content).
Rule of thumb: Add a series resistor (typically 33 Ω) close to the driver's output to reduce the rise- and fall-time.
Rule of thumb: The highest significant frequency content f_{max} [Hz] in a digital signal does not depend on the first harmonic (fundamental frequency). Instead, it depends on the rise- and fall-time:

$$f_{max} \approx \frac{0.35}{t_{10\%-90\%}} \tag{16.1}$$

where

$t_{10\%-90\%}$ = rise- and/or fall-time (whichever is smaller) from 10 to 90 % of the slope of a digital signal in [sec]

Rule of thumb: Every PCB trace of length longer than $\lambda/10$ [m] should be considered a transmission line and no longer as a simple interconnection (where λ [m] is the wavelength). This means that such a trace should be laid out with controlled impedance Z_0 [Ω]. In other words, avoid impedance changes or discontinuities along the PCB trace, as these impedance changes or discontinuities could lead to reflections or ringing. Reflections and ringing affect the signal integrity and lead to increased electromagnetic radiation.

16.8 Guideline # 7: Keep Clock lines As Short As Possible

Goal = reduced radiated emissions.
To paraphrase the honorable Henry W. Ott: "Get paranoid about clock routing!" [4]. Take care about clock lines and their return current paths and keep them as short as possible!

16.9 Guideline # 8: Fill Top and Bottom Layers with Circuit GND

Goal = reduced radiated emissions.
Fill the top and bottom layer of a PCB with a solid ground plane around the signals (copper area) and metalize the PCB edges (Fig. 16.3). This helps minimize radiated emission because the filled GND areas at the top and bottom layers shield inner-layer signals and prevent radiation. Moreover, the filled copper areas help maintain a low impedance return current path and short current loops.

Important: do not forget to place a grid of ground stitching vias throughout the whole PCB (otherwise, some small copper islands will start to radiate and you will get more radiation than without the solid copper fill)! This is very important! The rule of thumb in this section below presents a method of determining the maximum distance between stitching vias.

In addition, plated PCB outside edges (connected to circuit GND) help prevent the inner PCB layers from radiating. The plated PCB edges also help increase the cooling efficiency of a PCB because there is an additional copper surface where heat exchange can occur. The additional costs for metalized PCB edges are low.

Rule of thumb: When filling top and bottom layers with ground (copper pour), it is best practice to add a grid of ground stitching vias over the whole PCB. Otherwise, some small GND copper areas would tend to radiate! The distance between these vias within that grid depends on the highest frequency f_{max} [Hz] on the PCB. Given a signal with wavelength λ [m], it is a rule of thumb that a stub or trace of length $l \geq \lambda/10$ starts to become a problem (regarding radiation) and a trace of length $l < \lambda/20$ will not be a problem (in between $\lambda/10$ and $\lambda/20$ is a gray area [4]). Therefore, the distance between the vias should be shorter than $\lambda/10$ of f_{max} [Hz].

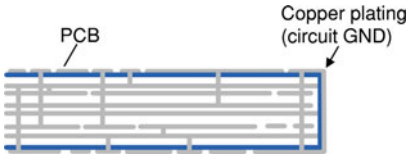

Fig. 16.3 Profile view of a multi-layer PCB with metalized edges

Table 16.1 $\lambda/10$ for a given frequency f_{max} [Hz] and PCB material with ε'_r

Smallest rise/fall-time on the PCB [nsec]	Highest frequency f_{max} on the PCB	$\lambda/10$ for ε_r=3,5 (**ceramic+PTFE**) [mm]	$\lambda/10$ for ε_r=4,5 (**FR-4**) [mm]	$\lambda/10$ for ε_r=6 (**HF-laminate**) [mm]	$\lambda/10$ for ε_r=11 (**HF-laminate**) [mm]
500	0.7 MHz	22908	20203	17496	12922
200	1.75 MHz	9163	8081	6999	5169
100	3.5 MHz	4582	4041	3499	2584
50.0	7 MHz	2291	2020	1750	1292
20.0	17.5 MHz	916	808	700	517
10.0	35 MHz	458	404	350	258
5.00	70 MHz	229	202	175	129
2.00	175 MHz	92	81	70	52
1.00	350 MHz	46	40	35	26
0.50	700 MHz	23	20	17	13
0.20	1.75 GHz	9.2	8.1	7.0	5.2
0.10	3.5 GHz	4.6	4.0	3.5	2.6
0.05	7 GHz	2.3	2.0	1.7	1.3
0.02	17.5 GHz	0.9	0.8	0.7	0.5
0.01	35 GHz	0.5	0.4	0.3	0.3

The wavelength λ [m] of a sinusoidal signal running through a PCB signal trace is according to Eq. 4.2:

$$\lambda = \frac{c}{f \cdot \sqrt{\varepsilon'_r}} \tag{16.2}$$

where

$c = 1/(\sqrt{\mu_0 \varepsilon_0}) = 2.998 \cdot 10^8$ m/s = speed of light
f = frequency of a sinusoidal signal in [Hz]
ε'_r = relative permeability of the PCB material (typical $\varepsilon'_r = 4.5$ for FR4)

However, how to determine f_{max} [Hz] or $\lambda/10$ [m], respectively? Usually, the highest frequency f_{max} [Hz] on a board can be found in the digital signals, e.g., the clock signals:

$$f_{max} = \frac{0.35}{t_{10\%-90\%}} \tag{16.3}$$

where

- $t_{10\%-90\%}$ = rise- and/or fall-time (whichever is smaller) from 10 to 90 % of the slope of a digital signal in [sec]

Table 16.1 shows example values of high-frequency digital signals rise-/fall-time, its corresponding highest frequency content f_{max} [Hz] and $\lambda/10$-values (as mentioned above, the recommended distance between the vias of the grid of vias is $< \lambda/10$).

16.10 Guideline # 9: Add Stitching Vias Around High-Speed Signal Vias

Goal = reduced radiated emissions.
Imagine the following scenario, a high-speed signal changes from one plane to another plane of a PCB. In order to minimize ground bounce, the return current path impedance should be minimized [1]. There are these two options, depending on the return current path:

1. **Identical return current reference nets.** If the two planes have the same reference net with identical electrical potential (e.g., GND), add two or three *stitching vias* (between the reference planes) close to high-speed signal via. These stitching vias help keep current loops and, therefore, the inductance as small as possible.
2. **Different return current reference nets.** If the two reference planes are DC isolated, ensure that the two reference planes are coupled with the lowest impedance possible. This can be achieved with the thinnest possible dielectric layer between them (see Fig. 16.4).

16.11 Guideline # 10: Add a Capacitor Close to Every Pin of a Connector

Goal = reduced radiated emissions, increased immunity.
Filtering of signals directly at the connector is very important! This helps increase ESD immunity to a PCB, reduce radiated emissions, and increase immunity to coupled burst signals on IO-cables. Every signal or power supply line which enters or leaves a PCB needs a filter element, e.g., a ceramic capacitor. One side of the capacitor should be connected close to the connector pin, the other pin tied to the ground plane with low inductance. Table 16.2 proposes some common capacitor values depending on the signal's data rate.
Hint: Signal lines which leave a device (e.g., a connector which people can touch with their hands) is exposed to ESD (±2 kV, ±4 kV, ±6 kV, ±8 kV). In this case,

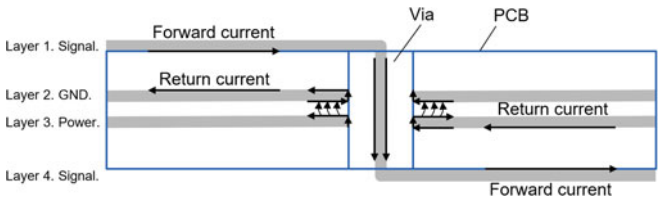

Fig. 16.4 Return current path in case of a reference plane change [1]

Table 16.2 Capacitors of IO-filters vs. data rate (rule of thumb)

Data rate	Rule-of-thumb for EMC, EMI, ESD capacitors as IO-filters
100 kBit/s	< 100 pF
1 MBit/s	< 22 pF
10 MBit/s	< 10 pF
100 MBit/s	TVS diodes with C < 1 pF
>1 GBit/s	TVS diodes with C < 0.1 pF

use capacitors with a high voltage rating (e.g., > 250 V, depending on capacitance and ESD test voltage and other components involved, e.g., like ferrite beads between connector pin and capacitor or conductor length).

16.12 Guideline # 11: Connect Circuit GND to Chassis at IO Area

Goal = reduced radiated emissions, increased immunity.
Bound a circuit GND to chassis at the area where a cable leaves/enters the chassis. Connect it with very low impedance! It is important that GND and chassis have the same potential in the IO area:

- It prevents unintended radiation, as the GND shows a minimum voltage difference to the chassis (earth).
- It makes the IO-signal filters on a PCB most effective and keeps ESD pulses away from the circuits on the board. Why? Because incoming noise and interference from the cable or connector can directly flow back to the source along chassis and earth.

16.13 Guideline # 12: Lay Cables Along Chassis (GND/Earth)

Goal = reduced radiated emissions.
Whenever possible, lay cables constantly along the chassis. This keeps the electromagnetic field generated by the voltages and currents in the cable at a minimum radiation level. The word *constantly* is essential because when laying out cables constantly along a chassis, there is no change in electrical balance (a change in electrical balance leads to common-mode currents) [3].

16.14 Guideline # 13: Don't Use Cable Shield as Signal Conductor for Low-Frequency Signals

Goal = increased immunity.
The cable shield should not be one of the signal conductors for low-frequency signals because of the potential interference with the ground loop current in the shield.
Hint: This rule does not apply for high-frequency signals, where the signal return current and the noise current are separated by the skin effect within the shield (return current of the high-frequency signal flows on the surface of the inner side of the shield and the noise current on the outer surface).

16.15 Guideline # 14: Cable Shield Grounding on Only One End for Low-Frequency Signals

Goal = increased immunity to electric-fields.
It may lead to problems when laying both ends of a cable shield to ground for low-frequency signals because ground loop currents in the shield could interfere with the signals inside the cable.
Rule of thumb: For shielding of low-frequency ($<100\,\text{kHz}$) signals:

- **Shielding against E-fields:** Lay only one end of the shield to ground (with low impedance) to avoid noise current through the shield (e.g., induced by magnetic fields or ground loop currents).
- **Shielding against H-fields:** Lying only one end of the shield to ground does not protect from H-field interference. If protection against low-frequency H-fields is needed, a shield with relative permeability $\mu_r' \gg 1$ is necessary. Twisting does also help to protect against H-field coupling.

If you are in control of only one side of the cable shield (because at the other end of the cable is an unknown device from various manufacturers), then lay the cable shield to ground with low inductance (no pigtails, use a 360° shield clamp) or implement a hybrid ground. A hybrid ground is a compromise for shielding against high-frequency signals, while minimizing low-frequency ground loop currents in the shield (see Sect. 13.7.4 and Fig. 16.5): Lay the cable shield to ground with a resistor (to reduce the ground loop current in the shield for low-frequency signals) and add a parallel capacitor to that resistor (to allow high-frequency signals to flow through the cable shield).

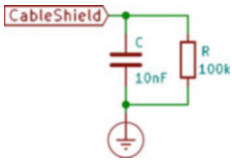

Fig. 16.5 Hybrid cable shield grounding

16.16 Guideline # 15: Cable Shield Grounding on Both Ends for High-Frequency Signals

Goal = increased immunity, reduced magnetic-field emissions.
It is a must to lay both ends of high-frequency signal cable shields to ground with low inductance (no pigtails, use a 360° shield clamp or the like).
Rule of thumb: For high-frequency (>1 MHz) signals:

- The shield can be used as signal return path for high-frequency signals, because the signal return current and the noise current are separated by the skin effect. The induced noise current in the shield helps to cancel out the magnetic field of the outside noise source.
- To reduce the magnetic field emissions from a signal in a shielded cable, the shield has to be laid on ground on both ends [4].

16.17 Guideline # 16: Minimize Loop Area of Signals in Cables

Goal = increased immunity to magnetic-fields.
The best way to protect a signal from magnetic fields is to reduce the current loop area A [m^2] [4]. Minimizing the loop area A [m^2] in case of a cable means twisting the wires of the forward and return current or using neighbor conductors for the forward and return current in flat ribbon cables.

16.18 Guideline # 17: Avoid Electrical Balance Changes

Goal = reduced radiated emissions.
A change from electrically balanced to unbalanced and vice versa (mode conversion) is called an electrical balance change (balanced and unbalanced transmission lines are topic in Sect. 7.9). Electrical balance changes lead to common-mode currents. And we do not want common-mode currents! Common-mode currents are often the cause for unintended radiated emissions. Thus, mode conversions should be avoided. The maximum common-mode voltage $V_{CM,max}$ [V] generated due to

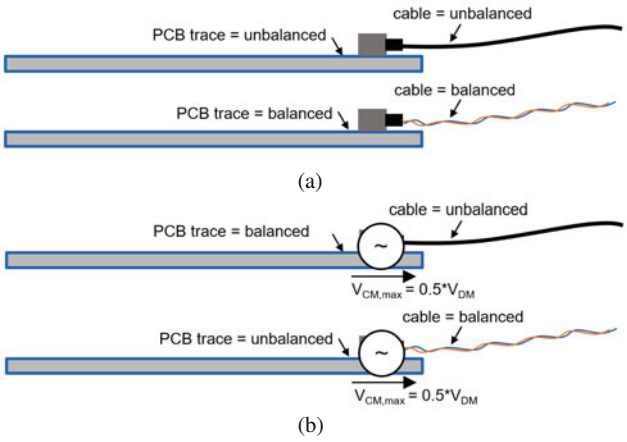

Fig. 16.6 Good and bad examples of PCB-to-cable-interconnections. (**a**) Good examples. (**b**) Bad examples

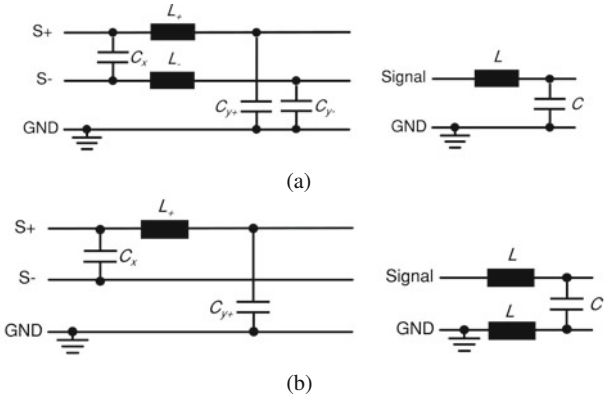

Fig. 16.7 Good and bad examples of how to filter balanced and unbalanced signal lines. (**a**) Good examples. (**b**) Bad examples

mode change is $V_{CM,max} = \Delta h_{max} V_{DM} = 0.5 V_{DM}$ [2], where h is the imbalance factor (Sect. 12.2.1) and Δh_{max} is the maximum imbalance factor change.

Avoiding electrical balance changes for cables connected to a PCB means:

- If the signal is balanced, stay balanced (twisted pair, flat cable). See Fig. 16.6a.
- If the signal is unbalanced, stay unbalanced (coaxial, multi-layer flat cable). See Fig. 16.6a.

Avoiding electrical balance changes for filters means:

- If a signal is balanced, add the identical filters to both signal lines. See Fig. 16.7a.
- If a signal is unbalanced, add only filters to the signal line. See Fig. 16.7a.

Rule of thumb: Send single-ended signals over unbalanced transmission lines and differential signals over balanced transmission lines. Balanced and unbalanced transmission lines are explained in Sect. 7.9 and single-ended and differential signal interfaces in Sect. 7.10.

References

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