

Low-Noise Mixed-Signal Electronics for Closed-Loop Control of Complex Photonic Circuits



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Abstract An increasing research effort is being carried out to profit from the advantages of photonics not only in long-range telecommunications but also at short distances, to implement board-to-board or chip-to-chip interconnections. In this context, Silicon Photonics emerged as a promising technology, allowing to integrate optical devices in a small silicon chip. However, the integration density made possible by Silicon Photonics revealed the difficulty of operating complex optical architectures in an open-loop way, due to their high sensitivity to fabrication parameters and temperature variations. In this chapter, a low-noise mixed-signal electronic platform implementing feedback control of complex optical architectures is presented. The system exploits the ContactLess Integrated Photonic Probe, a non-invasive detector that senses light in silicon waveguides by measuring their electrical conductance. The CLIPP readout resolution has been maximized thanks to the design of a low-noise multichannel ASIC, achieving an accuracy better than -35 dBm in light monitoring. The feedback loop to stabilize the behaviour of photonic circuits is then closed in the digital domain by a custom mixed-signal electronic platform. Experimental demonstrations of optical communications at high data-rate confirm the effectiveness of the proposed approach.

1 Introduction

The increasing demands in terms of bandwidth and energy efficiency required by telecommunications, automotive applications and datacenters are pushing copper-based interconnections close to their intrinsic limits [1]. In the same way, the new trends on rack-scale multi-processor computational units are putting pressure on chip-to-chip connections, calling for low-latency high-speed performance at reduced power and cost [2]. These technological requirements are making traditional interconnects the bottleneck of high-performance systems, suggesting the use of point-

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to-point optical connectivity not only for long distance communications but also at short range [3]. Compared to other solid-state solutions, Silicon Photonics (SiP) seems to be the ideal candidate to answer to these needs, sharing the same fabrication technology of the microelectronic industry.

Similarly to MEMS technologies, which exploited the mechanical properties of silicon to create a new family of devices and applications that are now supporting the electronic industry with a large fraction of its revenues [4, 5], Silicon Photonics is called to leverage the optical properties of silicon to create a new realm of miniaturized systems and devices and implement innovative functionalities. The silicon crystal is in fact transparent to near-infrared radiation, in particular to 1550 nm, which is the typical working wavelength of long-range fiber links, and to 1310 nm, which is of increasing interest for short-distance interconnects. Moreover, light confinement into a lithographed waveguide can be obtained by using silicon dioxide as cladding material, thanks to the large refractive index difference with respect to silicon. These features have already enabled the demonstration of high-complexity architectures integrating different kind of photonic devices, like Mach Zehnder interferometers (MZI), ring resonators, arrayed waveguide grating router (AWGR) [6, 7], allowing on-chip manipulation of light.

Even though photonic technologies have already demonstrated maturity for integrating lots of devices in a small footprint [8], the widespread use of complex silicon photonic architectures is still limited in real applications. The motivation for this delay is found in the inherent nature of photonic devices, that usually rely on interferometry and are thus very sensitive to fabrication tolerances, temperature variations and mutual crosstalk. As an example, the resonant frequency of a ring resonator filter is observed to move of 10 GHz due to 1 °C temperature change [9], making it very hard to reliably operate photonic architectures in harsh environments like datacenters without a real-time monitoring of their working conditions. Local light sensing, possibly with CMOS compatible detectors, and active control of each photonic element thus emerged as strong requirements to implement closed-loop stabilization and fully exploit the potential of photonic integration.

2 The Challenge of Transparent Detection

To reliably operate a complex photonic circuit, the working point of each integrated device needs to be assessed in real-time without changing its functionality. When the number of elements in a circuit is limited to a few units, light monitoring can be obtained by tapping a small part of the optical power from the waveguide towards a photodetector. The use of germanium photodiodes is the most common solution in this case [10, 11], even though the addition of this material to the technology is not trivial and it increases the final cost of the die. However, when the count of integrated devices in the chip increases to hundreds or thousands, this approach becomes rapidly unfeasible, as the large quantity of probing points causes an unacceptable light attenuation and/or perturbation [12].

For these reasons, a relevant research effort is being carried out to investigate the use of non-invasive in-line photodetectors, that exploit the waveguide itself as a light sensor and promise to allow the control of large-scale photonic circuits. Even though silicon is nominally transparent to near-infrared wavelengths, photocarrier generation has been observed in silicon waveguides because of two photon absorption (TPA) [13, 14] and sub-bandgap mechanisms such as surface-state absorption (SSA) [15, 16], that are responsible of the intrinsic propagation losses of photonic waveguides. Since the amount of free carriers generated by these mechanisms is small, transparent detectors usually have a lower sensitivity with respect to germanium photodiodes but, as they detect the full optical power in the waveguide and not just a small part of it, their use is not so disadvantageous compared to the standard approach.

Among the several solutions found in literature, the fully transparent ContactLess Integrated Photonic Probe (CLIPP) [17] was chosen in this work to monitor the state of complex photonic circuits. Like a photoconductor, this detector measures the changes of waveguide conductance caused by free carriers generation. However, to perform a truly non-invasive sensing, the core is not doped or processed and the access to its electrical properties is obtained capacitively, by adding two metal electrodes on top of the cladding 700 nm away from the core. Figure 1a shows a 3D picture of the CLIPP detector and its simplified electrical model. To effectively bypass the access capacitance C_A and read the electrical resistance of the waveguide R_{WG} , one electrode of the sensor is driven at a frequency $f_{CLIPP} > 1/\pi C_A R_{WG}$, usually between 100 kHz and 10 MHz depending on the pad geometry, while the other is connected to a TransImpedance Amplifier (TIA) to collect the current of the sensor and translate it into a voltage. A lock-in detection, achieved by demodulating the output of the TIA at the same frequency of the sensor stimulation, is thus a convenient readout scheme, allowing to reconstruct the complex admittance of the sensor and minimize the electronic noise at the same time. The readout noise is indeed of particular importance in this application. The conductance of the core is around 1 nS [17], so a resolution better than 1 pS is targeted to monitor the optical power in photonic devices with an accuracy below -30 dBm (Fig. 1b).

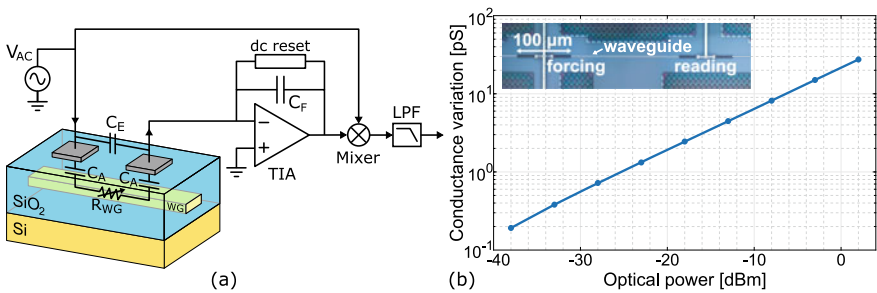


Fig. 1 **a** 3D representation of a CLIPP detector and its readout. **b** Sensitivity curve of a 400 μm device. Low noise readout is required to detect light variations below -30 dBm, corresponding to conductance changes < 1 pS

3 Integrated Lock-In Readout System

To perform an effective CLIPP readout with the best possible resolution, a multichannel lock-in based ASIC was specifically designed in STMicroelectronics BCD8sP 0.18 μm technology (Fig. 2) [18]. The design takes advantage of a capacitive-feedback TIA architecture to simultaneously achieve low noise and wide bandwidth. The front-end amplifier features a series white noise of only $2.8 \text{ nV}/\sqrt{\text{Hz}}$, with a corner frequency of 300 kHz, and a gain-bandwidth product of 2 GHz, reflecting in a closed-loop bandwidth around 80 MHz. The capacitive feedback, implemented with an inherently linear passive element, guarantees the required linearity over a rail-to-rail output.

Capacitive-feedback TIAs require a DC handling network to set the bias of the amplifier and discharge any leakage current coming from the sensor, that would otherwise cause the saturation of the output. This problem is of particular relevance in photonic applications, where the electronic front-end is used close to the photonic devices and light escaping from the optical circuit can cause photo-generated currents at the input of the TIA up to the nA range. To solve this issue, an active DC feedback network has been implemented. Here, the output voltage of the TIA is read by an auxiliary active circuit, which removes the AC signal and feeds the DC and low-frequency components back to the input node, effectively creating a DC handling mechanism. By using an integrator in the feedback path, this topology operates with a zero residual offset, apart from mismatch effects and non-idealities.

The overall gain of the readout circuit, which depends on the value of the feedback capacitance C_F and on the amplitude of the signal used to stimulate the CLIPP sensor, is ultimately limited by the value of the feedthrough capacitance C_E . To mitigate this issue and increase the maximum stimulation amplitude, a capacitance compensation system was added at the input of the chip. A programmable capacitor, tuned with a 4-bit digital-to-capacitance converter (DCC) and driven in counter-phase with respect to the stimulation of the sensor, is connected in parallel to the CLIPP to sink the

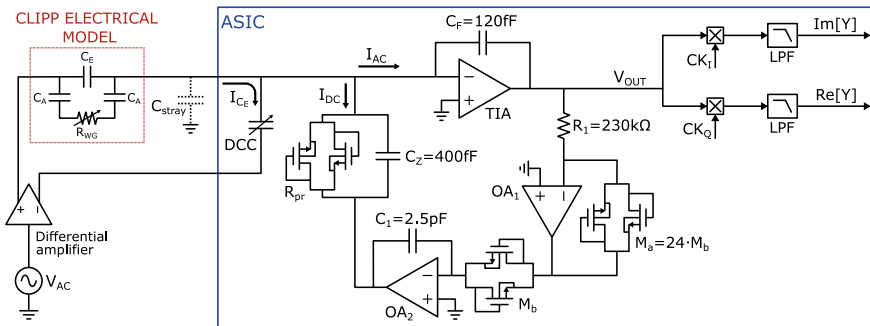


Fig. 2 Schematic of the 11-channel low-noise wide-bandwidth lock-in front-end ASIC, fabricated in 0.18 μm STMicroelectronics BCD8sP technology

spurious current injected by C_E . This solution allows to use stimulation signals as high as 10 V with a C_F of 120 fF, with great benefits in terms of readout resolution. Indeed the DCC, together with the input-referred current noise below $1 \text{ pA}/\sqrt{\text{Hz}}$, allows to achieve a resolution in the readout of conductance well below 1 pS. This extreme level of accuracy enables the detection of light variations below -35 dBm , suitable to control photonic architectures with the required precision.

4 Multichannel Electronic Platform for Closed-Loop Control of Photonic Circuits

The analog preamplification performed by the integrated front-end is complemented by an electronic system to reliably control the working point of photonic circuits. The system is designed in a modular way (Fig. 3) [19]: a first PCB, shaped to best fit in the optical bench, houses the photonic and electronic chips, while a larger motherboard hosts the rest of the electronics. This approach allows to maximize the readout accuracy by mounting the two chips close to each other, while allowing easy optical coupling and good flexibility in the design of the electronics.

The custom mixed-signal motherboard is designed to: (i) generate the sinusoidal signal necessary to drive the CLIPP, with tunable frequency (50 kHz–10 MHz) and amplitude (1–10 V) to adapt to different sensor geometries; (ii) amplify, filter and D/A convert the signal coming from 16 CLIPP detectors, without introducing any degradation in the readout resolution; (iii) drive up to 16 actuators on the photonic chip, with a voltage precision of few mV and maximum current of 50 mA; (iv) perform the feedback algorithms to control the working points of photonic devices.

The digital core of the system is an FPGA for real-time flexible parallel processing. The FPGA is housed in a commercial module, with all the components to connect it with a PC via USB. The FPGA handles the communication with all the components of the platform and generates the signals needed for the lock-in detection. To achieve the best possible resolution in the measurement, a heterodyne lock-in down-conversion is performed: a first analog mixer in the ASIC moves the signal to an intermediate frequency (f_{MID} , around some kHz) above the $1/f$ noise corner frequency of the acquisition chain, then, after digitization with the ADC, a second digital I/Q demodulation is done in the FPGA to down-convert the signal to baseband as required by the lock-in processing. A tunable digital filter sets the final readout bandwidth, which is defined based on the accuracy and speed requirements of the application.

The FPGA also implements the strategies to control the photonic devices. The operations can be divided into tuning, i.e. scanning the heaters voltage until the maximum or minimum of a desired cost function is reached, or locking, i.e. real-time feedback stabilization of the working point of a photonic device. Different control laws can be implemented and we successfully demonstrated integral and PI controllers [20], as well as gradient methods. The FPGA also generates modu-

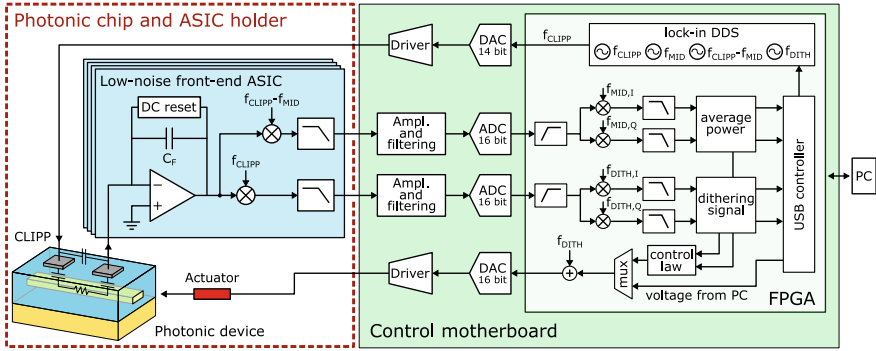


Fig. 3 Schematic view of the mixed-signal control platform for automated control of photonic circuits

lation tones (indicated as f_{DITH} in Fig. 3), which can be used for two reasons: (i) “labelling” each wavelength by modulating the input light source, to discriminate different signals in the optical architecture; (ii) using the dithering technique, by adding the tones to the heaters voltage to obtain a signal proportional to transfer function derivative of a photonic device, useful for power-independent locking [21]. A bank of additional lock-in mixers and filters is implemented in the digital domain for an efficient detection of these tones.

5 Experimental Demonstrations

An experimental demonstration of the full electronic system has been carried out with a photonic architecture conceived for intra-datacenter optical communications. The chip implements a low-energy any-to-any light router between N processing units, a very promising approach since it solves the radix-latency of switch-based solutions normally used to connect sockets inside datacenters. Each processor is equipped with a transmission engine (Tx), comprising $N-1$ lasers at different wavelengths that are combined on a single waveguide by an optical $(N-1):1$ multiplexer (MUX) to produce WDM-encoded data streams. Each data stream gets routed by the AWGR to the different receivers depending on its wavelength, with any-to-any transmission achieved thanks to the frequency routing of the AWGR. At the receiving end (Rx) of each socket, the data stream gets demultiplexed with a $1:(N-1)$ optical demultiplexer (DEMUX) so that each wavelength is acquired by a separate socket, allowing to discriminate the transmission from each sender.

To counteract any wavelength or thermal instability and safeguard the functionality of the WDM-based system in real datacenters environments, feedback stabilization is required. The resonant wavelength of the microring based structures inside the photonic chip was stabilized thanks to the dithering technique, that implements

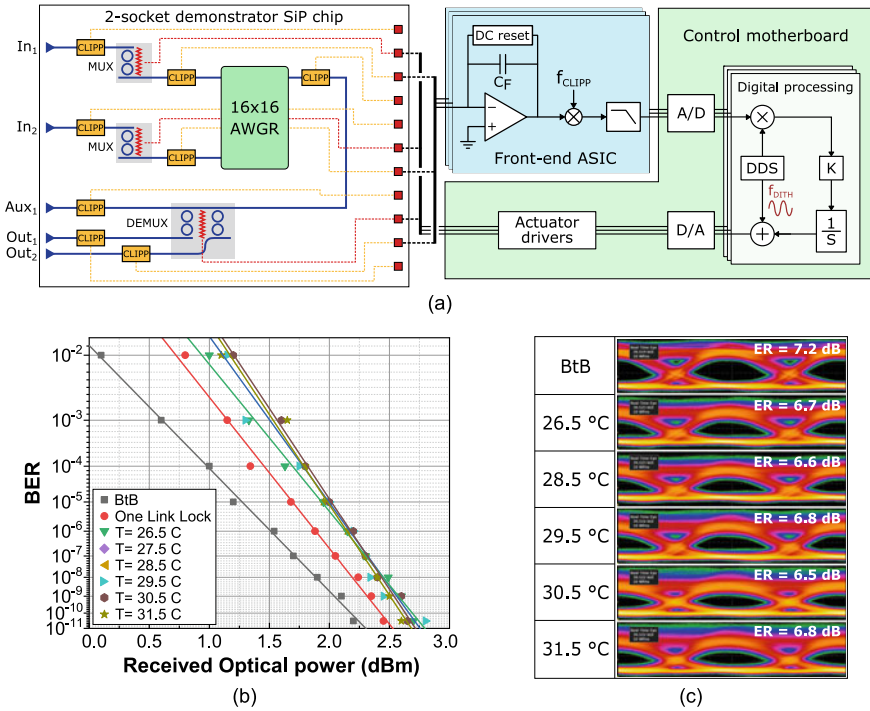


Fig. 4 **a** Silicon Photonic interconnection system integrated in a single chip and connected to the control electronics. **b** BER measurements and **c** eye diagrams at the output of the SiP chip, obtained at 30 Gbps at different temperatures

an easy yet effective power-and temperature-independent locking. To do so, a small sinusoidal signal is added to the MUX and DEMUX heater voltages, thus modulating the light in the output waveguide. The resulting light signal measured by the CLIPP is lock-in demodulated in the digital domain, obtaining, in this way, a voltage proportional to the first derivative of the transfer function of the device with respect to the temperature. Since the dithering signal is zero when the devices are at resonance, this information can be used as error signal to lock the rings.

The effectiveness of this approach has been experimentally demonstrated on a photonic chip featuring all the necessary building blocks to demonstrate optical communication between two transmitting sockets and a receiving one (Fig. 4a) [22]. A 30 Gbit s⁻¹ modulated laser signal was injected into the system and monitored at the output to obtain both eye diagrams and BER measurements, while a second laser served as a crosstalk source. To simulate the operation of the chip in a thermally unstable environment, temperature oscillations were intentionally generated in the setup. In these conditions, the electronic feedback control applies to the heater of

MUX and DEMUX a voltage that mirrors very precisely the temperature variations, effectively compensating any shift of the working point. This is proved by the transmission quality measurements performed on the output signal. Error-free operations at 5×10^{-11} error-rate were obtained during all the 20 min of the experiment and within 10 °C temperature range, with a maximum power penalty of around 1 dB when compared to the input signal (Fig. 4b). In addition, the crosstalk effect induced by the second optical signal resulted to be negligible on the transmission quality (power penalty lower than 0.4 dB). The same is confirmed by the eye diagrams, that retain an extinction ratio (ER) larger than 6.5 dB in all the explored conditions (Fig. 4c).

6 Conclusions

This chapter presented and discussed how to reliably operate complex silicon photonic architectures through the implementation of a robust electronic feedback control. To guarantee scalability to the system, the non invasive nature of CLIPP detectors was exploited to monitor multiple photonic devices simultaneously without impairing the overall optical functionality. A complete low-noise mixed-signal electronic system was then designed to read the detectors with maximum accuracy and close the feedback loop in the digital domain, allowing great flexibility in the implementation of the feedback strategy. The effectiveness of the control system was demonstrated with error free routing and transmission of a 30 Gbit s⁻¹ optical signal through a WDM-based routing engine. The result highlights that a proper electronic control layer can unlock the true potential of integrated optics and allow large-scale diffusion of this technology in real applications, paving the way to new sophisticated functionalities and architectures.

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