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Solder Joint Technology

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Abstract

This chapter introduces the key functions of solder joints and the various soldering processes. The evolution from leaded to lead-free solder materials is reported. Furthermore, the recent developments of high-temperature solders and composite solders due to the ever demanding functional and service requirements are discussed. The properties of different solder materials and their solder joints are also presented. Finally, reliability studies of the solder materials and their solder joints are discussed in terms of mechanical behavior, temperature cycling, and drop impact.

Introduction

Solder material serves as an electrical and mechanical interconnect in electronic packaging. Interconnects in electronic packaging are generally categorized into three levels. The zeroth level is an interconnect on the silicon itself which is made during wafer processing. This level of interconnect will not be discussed in this chapter as it does not involve the solder material. Level one interconnects are made between the die and the substrate and generally form the package. Some examples of these interconnects include C4 (controlled collapse chip connection) solder joints and wirebonding. Level two interconnects are joints between the substrate and the PCB (printed circuit board). These hold the package to the PCB. Examples of these include BGA (ball grid array) solder joints and leaded package soldering.

In the following sections, the key solder joint technologies (like surface mount technology, pin-through-hole technology, and flip chip technology) are briefly described. This chapter also presents the various soldering processes and the evolution of solder materials. Emphasis is also placed on how material characteristics of solder impact the solder joint performance. Reliability studies in terms of mechanical behavior, temperature cycling, and drop impact are also discussed.

Surface Mount Technology (SMT)

In most portable electronics such as mobile phones, SMT packages are very common as the manufacturing process for this is very mature, thus making them relatively cheap to manufacture. In SMT packages, the silicon (Si) die is wirebonded to the leadframe. However, there are limitations on the length of wirebonds as longer wirebonds are more susceptible to wire sweep during the encapsulation process. Wire sweep is said to have occurred when adjacent wirebonds move and come into contact, resulting in short circuit. To prevent this, wirebond pads are generally located at the periphery of the die. The legs of the leadframe can be bent into gull wings or J-wings and are

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placed onto the bond pads of the PCB which has solder paste printed on it. This assembly is subjected to the reflow process, resulting in the formation of solder joints. A schematic diagram of the leadframe package mounted on PCB using the SMT is shown in Fig. 1.

Pin-Through-Hole Technology

Pin-through-hole technology is another kind of second-level interconnection. In general, it has better mechanical reliability than SMT, however it is more expensive. It is used on leadframe packages with the legs bent straight as shown in Fig. 2. Holes are drilled on the PCBs and are plated with Cu and immersion Sn. Following this, the leadframe package is placed into the holes and it undergoes a wave soldering process such that the solder rises through the holes, connecting the leadframe legs to the PCB.

Flip Chip Technology

Flip chip technology is used in higher-end devices such as CPUs and server products. This type of interconnection is largely preferred due to the large number of I/Os present in these products and short interconnect length, which results in superior electrical performance. This technology involves the active Si surface being flipped over such that it faces the surface of the substrate. An area array of under bump metallization (UBM) is fabricated during wafer processing over the active circuitry of the silicon. Solder can be either electroplated or printed on the UBM. Other than a narrow keep-out zone at the edges of the die, these solder bumps cover the entire surface of the chip. Joints formed using this technology are referred to as C4 (controlled collapse chip connection) joints. This is because wetting can occur only on the UBM and not on the surrounding SiO_2 passivation, thus effectively controlling the height of joint. A schematic diagram of this package assembly is shown in Fig. 3.

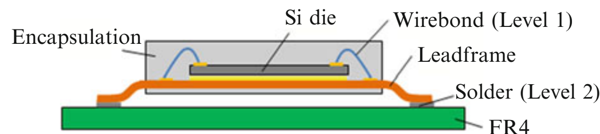

Fig. 1 A leadframe package mounted on board using SMT. Schematic diagram showing the cross-sectional view of a lead soldered to the copper pad of a PCB

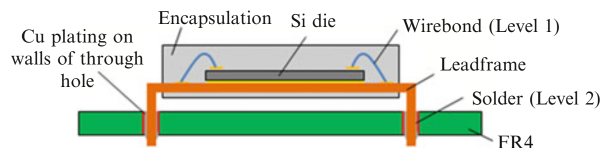

Fig. 2 A schematic diagram showing a leadframe package mounted on board using pin-through-hole technology

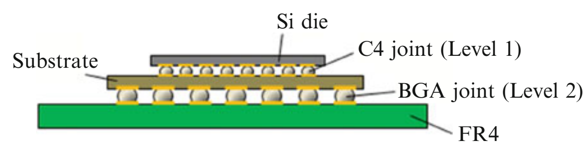

Fig. 3 Schematic diagram of a BGA package

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Besides the C4 joints, ball grid array (BGA) solder joints also undergo flipping during its manufacturing process. Unlike C4 joints, BGA joints are second-level joints. First, the solder balls are attached to the package. To do this, the package is flipped over and solder balls are placed on the pads of the package and undergoes a reflow step. Then the package is flipped onto the PCB, and the whole assembly is subjected to reflow again.

Metallurgical Reaction During Soldering

During soldering, the solder material is joined together without the need to melt the base metal (substrate). However, in order to achieve a reliable solder joint, a proper metallurgical bond between the two metal surfaces must be formed and wetting must take place. In general, wetting is said to happen if the wetting or contact angle lies between 0° and 90°. Conversely, if the contact angle lies between 90° and 180°, the system is considered to be non-wetting. According to Young's equation (Jacobson and Humpston 2004), the contact angle (θ_c) is determined from the balance of interfacial tensions at the junction, as shown in Fig. 4:

$$\gamma_{SF} - \gamma_{SL} = \gamma_{LF} \cos\theta_c \tag{1}$$

where γ_{SF} is the interfacial tension between the flux and solid base metal, γ_{SL} is the interfacial tension between the molten solder and the solid base metal, γ_{LF} is the interfacial tension between the molten solder and the flux, and θ_c is the contact angle. Figure 4 shows the spreading of molten solder on the horizontal and vertical surfaces. Superior wetting is associated with a small contact angle. In order to reduce the contact angle, it is useful to reduce γ_{LF} through the application of active flux.

The formation of a solder joint is made possible by (i) introducing fluxing agents to remove the oxide layer present on metal surfaces and (ii) using an inert environment during the soldering process, to reduce the oxide formation. Figure 5 shows the phenomena taking place during the

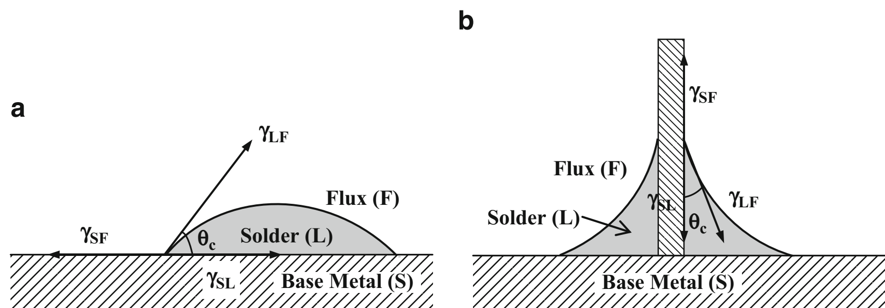

Fig. 4 Schematic diagrams showing the spreading of solder on (**a**) horizontal and (**b**) vertical surfaces. The contact angle (θ_c) is an indicator of wettability

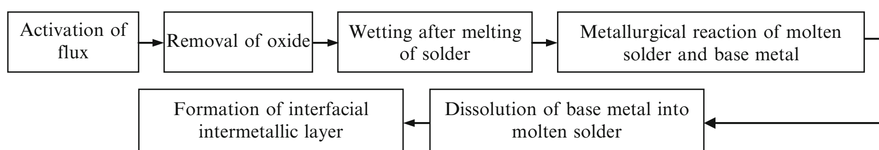

Fig. 5 Schematic diagram showing the various phenomena taking place during the soldering process

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soldering process. Upon the activation of the flux, the presence of oxide on the solder and base metal surfaces is removed. This allows wetting to take place as the solder melts. A metallurgical reaction of the molten solder and base metal occurs, and there is dissolution of the base metal into the molten solder. This reaction is known as liquid solder reaction, and it leads to the formation of an interfacial intermetallic layer. After the solidification of the solder joint, metallurgical reaction continues to take place while the joint is in service, and the reaction is termed as solid-state reaction.

As shown in Figs. 6 and 7, intermetallic compounds (IMCs) are formed at (i) the interface between solder and base metal of the substrate and (ii) inside the bulk solder material. The formation of such intermetallic compounds can alter the microstructure of the solder joints and hence influence their long-term reliability. Although the presence of interfacial IMCs is desirable for the formation of a good solder joint, studies have shown that excessive intermetallics growth degrades interfacial integrity (Ahat et al. 2001; Nai et al. 2009).

Soldering Processes

The soldering processes can be broadly classified into two groups, namely, (i) total heating method and (ii) partial heating method. Figure 8 shows the various soldering processes under each group.

For total heating modes, the entire package and/or printed wiring board is subjected to heat (refer to Fig. 9). It is widely used in the industry for large-volume production. It is efficient in terms of productivity and is economical. However, heat stresses are induced on the whole device and printed wiring board. On the other hand, for partial heating modes, heat is applied to the package leads

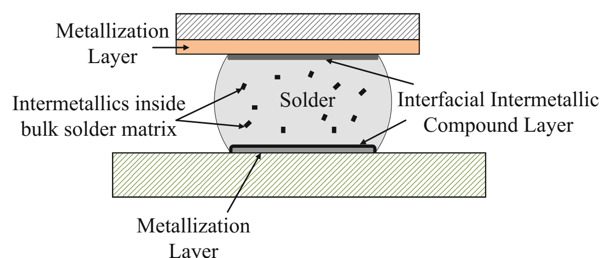

Fig. 6 Schematic diagram showing the cross section of a typical solder joint

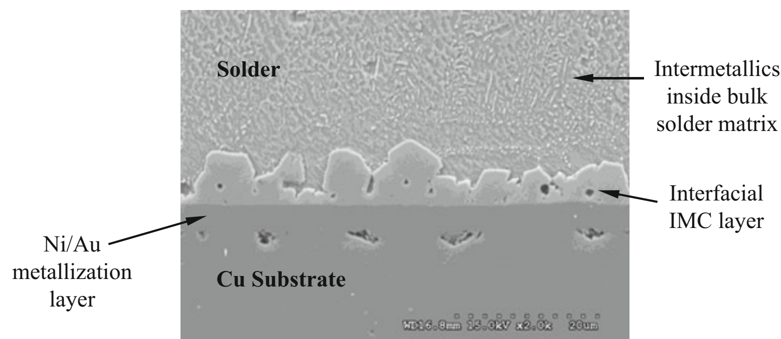

Fig. 7 Representative FESEM (field emission scanning electron microscopy) image showing the presence of interfacial IMC layer and intermetallics inside the solder matrix

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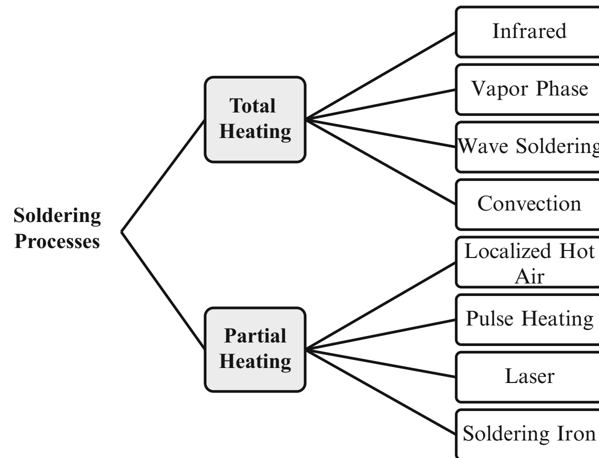

Fig. 8 Classification of soldering processes

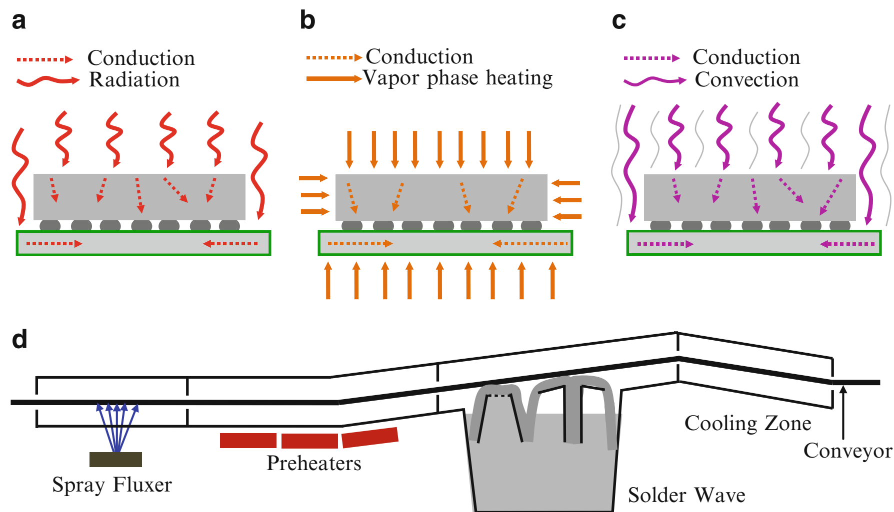

Fig. 9 Schematic diagrams showing the various total heating methods: (**a**) infrared mode, (**b**) vapor phase heating mode, (**c**) convection mode, and (**d**) wave soldering

and/or printed wiring boards in a localized manner (refer to Fig. 10). Though less heat stress is induced on the device and printed wiring boards, it is not ideal for large-volume production.

Solder Materials

Drive Towards Lead-Free Solders

The implementation of legislative and regulatory actions to restrict the use of lead (Pb) and Pb compounds has moved the electronics industry to do away with Pb in solder materials. In the electronics industry, the concerns over the use of Pb are from the occupational exposure, disposal of electronic assemblies which contain Pb and Pb waste derived from the manufacturing processes. There have been many studies on lead-free alternative solders in the past decade (Bieler and Lee 2010; Puttlitz and Stalter 2004; Chidambaram et al. 2011). These solder alloys can be broadly classified into (i) binary, (ii) ternary, and (iii) quaternary alloys. Majority of these solder alloys are

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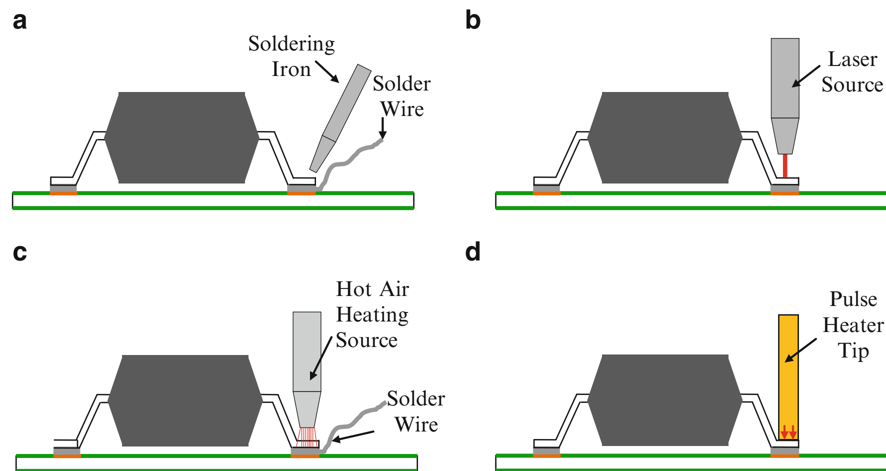

Fig. 10 Schematic diagrams showing the various partial heating methods: (**a**) soldering iron, (**b**) laser soldering, (**c**) localized hot air soldering, and (**d**) pulse heating

based on tin (Sn) being the primary or major constituent. In the following section "Characteristics of Bulk Solder and Solder Joints", the characteristics of these lead-free solder alloys will be presented in greater detail.

High-Temperature Lead-Free Solders

In the past decade, there has been momentous research effort in the development of lead-free solders. However, a limited portion of these is related to lead-free high-temperature solder alloys. In the field of high-temperature applications (e.g., deep well oil and gas logging tools, automotive under the hood electronics and aerospace electronics), there is an urgent need for such high-temperature lead-free solder alloys. In order to ensure efficient process control of the manufacturing and assembly of the soldered components, the melting range of the high-temperature solder alloys has been defined by the industry as 270–350 °C (Chidambaram et al. 2010).

The conventional high-temperature solders used include (i) Pb–Sn alloys which contain high amount of Pb (Nousiainen et al. 2006; Kim et al. 2003), (ii) Pb–Ag, (iii) Sn–Sb, (iv) Au–Sn, and (v) Au–Si alloys (Suganuma et al. 2009; Zeng et al. 2012). Table 1 lists some of the typical high-temperature solders, namely, high Pb solders, Au-based solders, Sn–Sb solders, Zn-based solders, and Bi–Ag solders.

Composite Solders

Stricter functional and service requirements of electronic devices, coupled with concurrent advances in the electronics industry towards miniaturization of devices, have necessitated for solder joints having enhanced mechanical, thermal, and electrical properties. The search beyond the conventional solders has led to the development of a new generation of interconnection material. A potentially viable way to effectively increase the service temperature capabilities and thermal stability of the base solder materials is the development of composite solders. Composite solders are solder alloys with intentionally added reinforcements.

To date, researchers have worked with a variety of reinforcement filler materials to synthesize composite solders (Nai et al. 2006, 2008a, b, 2009; Guo et al. 2001; Guo 2007; Liu et al. 2008; Babaghorbani et al. 2009; Shen and Chan 2009; Geranmayeh et al. 2011; Niranjani et al. 2011; Han et al. 2011, 2012; Tsao et al. 2012; Han et al. in press). The filler materials used can be classified into (i) elemental metallic particles, (ii) intermetallic particles or intermetallics formed from elemental

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Table 1 Lists of typical high-temperature solder alloys (Nousiainen et al. 2006; Kim et al. 2003; Suganuma et al. 2009; Zeng et al. 2012)

Alloys	Composition (wt.%)
Pb–Sn	Sn–65Pb
	Sn–70Pb
	Sn–80Pb
	Sn–90Pb
	Sn–95Pb
	Sn–98Pb
Pb–Ag	Pb–2.5Ag
	Pb–1.5Ag–1Sn
Sn–Sb	Sn–5Sb
	Sn–3Sb
Au–Sn	Au–20Sn
Au–Si	Au–3.15Si
Au–Ge	Au–12Ge
Bi–Ag	Bi–2.5Ag
	Bi–10Ag
	Bi–11Ag
Zn–Al	Zn–6Al
	Zn–4Al–3 Mg–3.2Ga
Zn–Sn	Zn–20Sn
	Zn–30Sn
	Zn–40Sn

particles through a reaction with Sn during manufacturing or by subsequent aging and reflow processes, and (iii) phases that have low solubility in Sn or are nonreactive with Sn. The filler materials used also varied in (i) size (e.g., micron, submicron, and nanoscale) and (ii) shape (e.g., particles, wires, and nanotubes).

With the advancement of nanotechnology in recent years, various nano-size reinforcements are chosen to synthesize the nano-composite solders. These nano-composite solders are developed primarily to enhance the service performance of solder joints, in particular their creep and thermomechanical fatigue resistances. Studies have shown that the nano-size reinforcements are preferred over their micron-size counterparts as they could more effectively distribute along the Sn–Sn grain boundaries and thus act as obstacles to restrict dislocation motion and limit grain boundary sliding (Shen and Chan 2009). In the case of nano-composite solders, other reported enhancements include (Shen and Chan 2009) (i) reduction in solder's density, (ii) reduction in the degree of undercooling, (iii) improvement of electrical conductivity, (iv) improvement of wettability of solders on substrates, (v) suppression of the growth of intermetallics (in terms of interfacial intermetallic compound layer growth and growth of intermetallics inside the solder matrix), (vi) refinement of microstructure (in terms of finer grains), and (vii) improvement of mechanical properties (in terms of microhardness, 0.2 % yield strength, ultimate tensile strength, shear strength, and creep resistance).

In general, composite solders with improved performance have been broadly demonstrated, although the technology is still embryonic and there are technical issues to be resolved before

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adoption by the industry. Nonetheless, there is keen industry interest, particularly how production of such materials might be cost-effectively adapted to real-life industry processes.

Characteristics of Bulk Solder and Solder Joints

In general, solder materials serving as interconnections need to provide the necessary mechanical, thermal, and electrical integrity in electronic assemblies. As there is a wide range of service requirements for solder materials, it is essential to understand the performance characteristics of the solder materials. These performance characteristics can be broadly grouped into (i) properties pertinent to reliability and (ii) properties pertinent to manufacturing. Figures 11 and 12 show the key properties of bulk solder material and their solder joints which are critical to reliability and manufacturing respectively.

Melting Temperature/Range

The melting temperature of solder materials is a critical property which is closely linked to the manufacturing process and the ability of the solder interconnect to withstand the service temperature. The melting temperature of Sn–Pb solder is 183 °C. Most of the assembly equipment previously used for Sn–Pb solder technology is designed to operate using 183 °C as a reference.

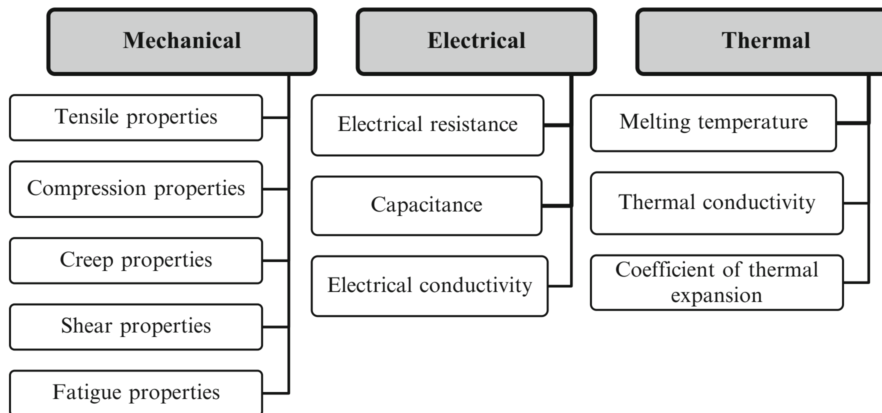

Fig. 11 Key characteristics important to reliability of bulk solder materials and their joints

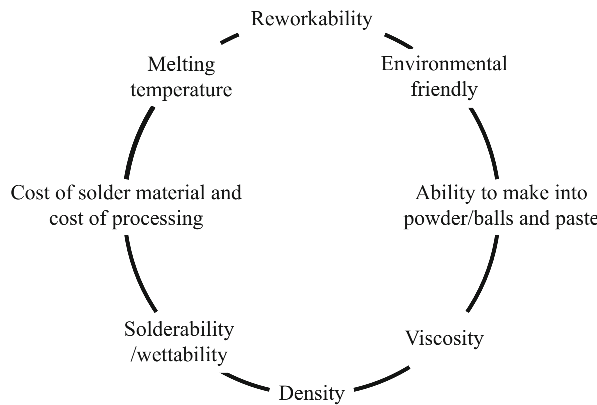

Fig. 12 Key characteristics important to manufacturing of bulk solder materials and their joints

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Table 2 List of lead-free solder selection and their melting point/range (Abtew and Selvaduray 2000; http://www.kester.com/SideMenu/LeadFreeSolutions/tabid/145/Default.aspx. Accessed 28 Sept 2012; Ganesan and Pecht 2006; Mahidhara 2000)

Solder alloy composition	Melting point/range °C
Au20Sn	280
Sn–5Sb	236–243
Sn–3Sb	232–238
Sn2.0Cu0.8Sb0.2Ag	219–235
Sn25Ag10Sb	233
Sn	232
Sn0.7Cu	227
Sn2.5Ag0.8Cu0.5Sb	217–225
Sn4.0Ag0.5Cu	217–224
Sn3.9Ag0.6Cu	217–223
Sn–3.5Ag	221
Sn2.5Ag1.0Bi0.5Cu	214–221
Sn–3.5Ag3Bi	220
Sn–3.0Ag–0.5Cu	217–220
Sn–2.0Ag–0.75Cu	217–219
Sn3.8Ag0.7Cu	217–219
Sn–3.5Ag0.7Cu	217–218
Sn2.5Ag0.8Cu0.5Sb	213–218
Sn2.0Ag3.0Bi0.75Cu	207–218
Sn–3.5Ag0.9Cu	217
Sn2Ag4Bi0.5Cu0.1Ge	216
Sn–3.5Ag5Bi0.7Cu	210–215
Sn2Ag3Bi0.75Cu	210–215
Sn4.0In3.5Ag0.5Bi	210–215
Sn8.0In3.5Ag0.5Bi	197–208
Sn9Zn	199
Sn8Zn3Bi	191–198
Sn20In2.8Ag	175–187
Sn57Bi0.1Ag	138–140
Sn58Bi	138
Sn52In	118

Table 2 lists the melting points of some solder materials. Although some variations in the baseline temperature can be accommodated by the equipment currently in use, if the melting point of the alternative solder is significantly higher, the existing processing equipment will have to be replaced. This will result in expensive investment of new equipment which will then translate to an increase in overall product cost. In addition, in an electronic assembly, a variety of materials is used. Particularly, there are many polymeric materials found in a typical electronic package, and these materials might not be able to tolerate the higher manufacturing process temperature.

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Table 3 Electrical resistivities of some solder alloys and microelectronic packaging materials (Abtew and Selvaduray 2000; Hwang 1996; Gray 1957; Lee et al. 1995; Kang et al. 1999)

Type	Materials	Resistivity (μΩ cm)
Solder alloys	Sn–37Pb	14.5
	Sn–2.8Ag–20In	17
	Sn–3.5Ag	10
	Sn–3.5Ag–0.7Cu	13
	Sn–3.8Ag–0.7Cu	13
	Sn–3Ag–5Bi	11.6
	Sn–3Ag–10Bi	8.8
	Sn–3Ag–3In	7.7
	Sn–3Ag–5Sb	10.5
	Sn–3Ag–1Zn	10.4
	Sn–3Ag–3Zn	4.8
	Sn–5Bi	11.0
	Sn–10Bi	17.7
	Sn–5In	8.3
	Sn–52In	14.7
	Sn–5Sb	17.1
	Au–20Sn	16
Leadframes	52Ni–48Fe	43.2
	42Ni–58Fe	57.0
Metallic elements	Ag	1.47
	Al	2.83
	Au	2.44
	Bi	119
	Cu	1.73
	In	8.37
	Mo	5.14
	Ni	7.24
	Pd	10.21
	Pt	7.83
	Sb	37.1
	Sn	11.5
	Zn	5.75

Electrical Properties

Solder serves as an electrical interconnect in devices whereby electrical currents flowing into and out of the device need to pass through the solder joints. In order to ensure proper functioning of the interconnect, the electrical resistivity of the solder materials has to be low so as to allow efficient current flow. For a given alloy material, the resistivity value varies with temperature, composition, and microstructure. Table 3 shows the electrical resistivities of some solder alloys and microelectronic packaging materials.

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Table 4 Thermal conductivity values of solder alloys and microelectronic packaging materials (Suganuma et al. 2009; Abtew and Selvaduray 2000; Hwang 1996; Lee et al. 1995; Bilek et al. 2004; Hwang 1994)

Materials	Thermal conductivity (W/m•K) at 300 K
Ag	429
Au	297
Bi	8
Cu	401
Ni	91
In	82
Si	82
Sn	73
Sb	24
Al_2O_3	21
SiC	210
AlN	250
Sn–37Pb	50.9
Sn–3.5Ag	54.3
Sn–2.8Ag–20In	53.5
Sn–3.5Ag–0.9Cu	~60
Sn–3.8Ag–0.7Cu	
Au–20Sn	57
Au–12Ge	44
Au–3Si	27
Sn–5Sb	48
Pb–5Sn	23
Sn–0.7Cu	65

Thermal Conductivity

When electronic devices are in service, heat is generated by the die. For proper and long-term reliable functioning of the device, it is vital to ensure efficient heat dissipation from the die to the surroundings through its packaging. One of the heat dissipation pathways is through the solder interconnections. In the case of high interconnect ball grid array (BGA) devices, thermal solder balls which have no electrical connections are introduced to function as a heat dissipation medium. Table 4 lists the thermal conductivity values of some solder alloys and microelectronic packaging materials.

Coefficient of Thermal Expansion (CTE)

An electronics assembly comprises of many different materials which ranges from metals, ceramics, polymers, to composites. The whole assembly will experience thermal cycling when the device is in operation. These materials with different coefficients of thermal expansion (CTE) will expand and contract at different rates, resulting in thermally induced stresses during the thermal cycling of the device. Table 5 summarizes the CTE values of some solder alloys and microelectronic packaging materials.

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Table 5 CTE values of solder alloys and microelectronic packaging materials (Suganuma et al. 2009; Abtew and Selvaduray 2000; Hwang 1996; Hwang 1994; Handbook Committee 1989; Korhonen et al. 1993; Spearing et al. 1993)

Materials	CTE ($\times 10^{-6}$/K)
Si	3.0
SiC	3.7–3.8
Al_2O_3	7.0
AlN	4.03
FR-4; $T < T_g$	x, y: 15.8
FR-4; $T < T_g$	z: 80–90
FR-4; $T > T_g$	x, y: 20
FR-4; $T > T_g$	z: 400
Epoxy resins	~50
Bi	13.4
Cu	16–18
In	32.1
Sb	11.0
Sn	22.0
Sn–37Pb	21
Sn–3.5Ag	22
Au–20Sn	16
Au–12Ge	13
Au–3Si	12
Sn–5Sb	23
Pb–5Sn	30
Sn–4.8Bi–3.4Ag	23

Mechanical Properties

Solder interconnects not only conduct current, they also provide mechanical support for electronic devices. Thus, the mechanical properties of the solder materials used to form the solder joints are vital to the mechanical reliability of the devices. The three key mechanical properties of solders are, namely,

(i) Strength and stiffness
(ii) Creep resistance
(iii) Fatigue resistance

Under various service conditions such as temperature cycling, vibration during transportation, and drop impact conditions, the solder joint experiences tension, compression, and shear stresses.

Shear Mode

While an electronic device is in operation, the solder joints are subjected to mechanical stresses and strains due to the mismatch of coefficients of thermal expansion (CTE) between the different materials. Components in devices are made up of a variety of materials which have different coefficients of thermal expansion. When the device is switched on and off, it experiences thermal cycling and this leads to shear stresses as schematically illustrated in Fig. 13.

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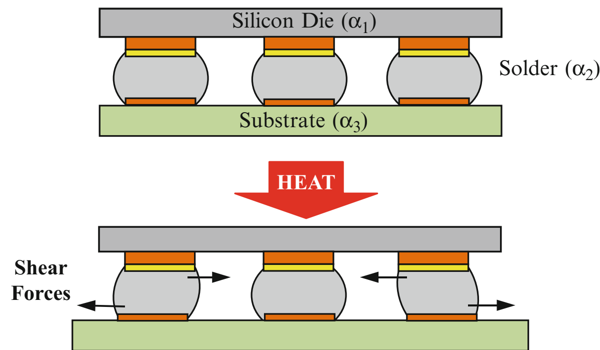

Fig. 13 Solder interconnects subjected to shear stresses during thermal cycling, due to CTE mismatch between the die (α1), solder (α2), and substrate (α3). α denotes the CTE of the material

Tension Mode

It is also of interest to determine the extent of tensile deformation the solder joints can endure without failure as they can be subjected to tensile loading during the handling of electronic devices. The tensile properties of a solder material can be derived from a stress–strain curve which consists of an elastic region and a plastic region. The elastic modulus (*E*, Young's modulus) can be determined from the slope of the elastic region of the curve. Within this elastic region, the sample will return to its initial dimensions when the applied load is removed. When the applied load increases and exceeds that of the elastic limit, the solder material will undergo plastic deformation whereby the deformation in this region is permanent. The 0.2 % yield stress (0.2 % YS) of the solder material is described as the level of stress resulting in the onset of plastic deformation. It is determined by drawing a parallel line to the slope of the elastic region at 0.2 % of the strain. Under tensile loading, the maximum level of stress which the solder material can endure before failure is defined by the ultimate tensile stress (UTS).

Creep

Creep deformation is a key failure mode of solders due to the high homologous temperature of solder materials. The homologous temperature (T_h) is defined as the ratio of the temperature of the solder material and its absolute melting temperature, T_m (in degrees Kelvin) (Callister 2007). When T_h is greater than 0.5 T_m, the creep deformation will be the dominating mode of deformation in metallic materials. For most solder alloys, even at room temperature, the homologous temperature is greater than 0.6 and this leads to the solder joints being loaded under conditions whereby they are prone to creep.

Creep is a time-dependent plastic deformation under a constant stress in either tension or compression. A typical creep curve is made up of three stages as shown in Fig. 14. The first stage is the primary creep where the strain rate decreases rapidly over time due to work hardening which restricts the deformation. The second stage is the secondary creep, also known as the steady-state creep region. This stage is the most vital as deformation of the solder materials dominates here. Most of the published literature is on steady-state creep. The final stage is the tertiary creep where the creep strain rate increases rapidly over time and will result in creep rupture of the testing sample.

Fatigue

Due to mechanical or thermal cyclic loading, solder joints are also susceptible to fatigue failure. This type of solder joint failure can lead to (i) crack nucleation and (ii) microcrack propagation and

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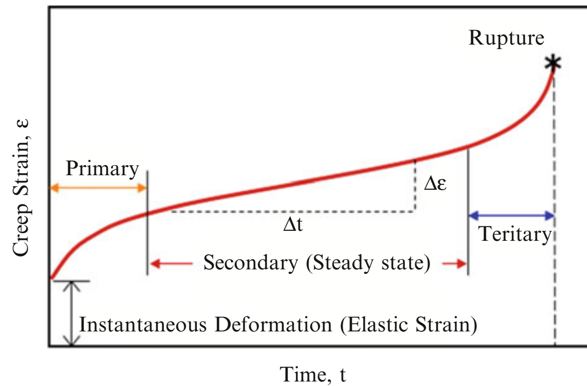

Fig. 14 Graphical representation of a typical creep curve showing the three key stages

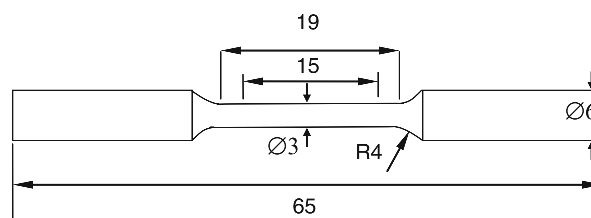

Fig. 15 Typical dimensions of a bulk solder sample used for mechanical testing (Pang 2012)

coalescence (Fine 2004). The fatigue life of a solder joint is determined by the number of stress cycles it can withstand before electrical failure occurs.

Samples Used for Mechanical Testing

For mechanical design, modeling, life prediction, reliability assessment, and process optimization, it is critical that the properties of the solder material must be reliable and accurate. However, there are discrepancies in the mechanical property database of solder materials due to the absence of uniformity in testing standards. Furthermore, there is a lack in correlation between the bulk solder properties and that of soldered joints.

Solder used in electronic industry exists in various forms: (i) solders for operations such as wave soldering, (ii) solder paste for operations such as surface mount reflow, and (iii) solder balls or solder columns for applications such as ball grid array, column grid array, and flip chip packages. The design of test specimen thus plays an important role in the representation and validity of the testing result. The specimens currently used to determine the mechanical properties of solder interconnect can be grouped into (i) bulk solder, (ii) simplified shear sample, and (iii) surface mount technology (SMT) solder joints.

In general, bulk solder specimens, as shown in Fig. 15, can be used to determine the mechanical properties of solder alloys (Pang 2012). However, such testing specimens could not accurately model the service life of an actual electronic assembly due to the size effect. Hence, Darveaux and Banerji (1992) used solder assemblies for mechanical testing. The size of the test specimens was very close to the actual soldered assemblies. Figure 16 shows some mechanical test specimens which are better representatives of the actual solder interconnects (Plumbridge 2004).

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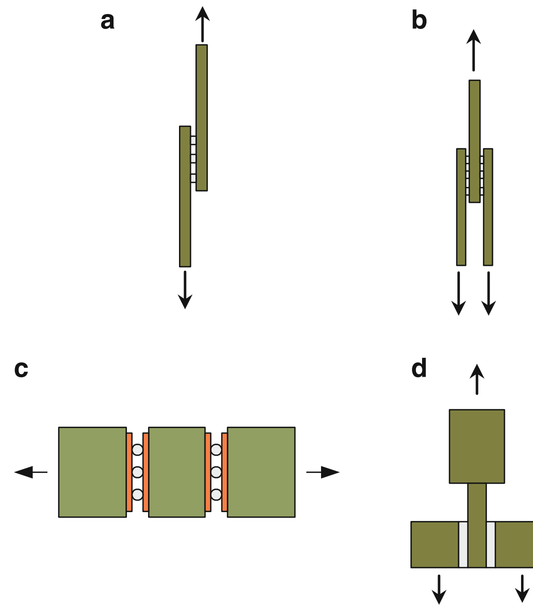

Fig. 16 Schematic diagrams of different test specimens used for mechanical testings. (**a**) Single lap shear, (**b**) double lap shear, (**c**) solder ball tension, and (**d**) ring pin shear

Reliability Case Studies

Mechanical Study of Bulk Solder

With the rapid progress in technology, our everyday life becomes more dependent on electronics. Hence, the research in the dynamic response of solder interconnects to make these electronic devices more robust becomes crucial. Accurate material models and test results allow the effective comparison and selection of suitable solder materials for various application needs and in extracting mechanical parameters required for finite element modeling. The study by Ong (2005) to obtain the properties of Sn–37Pb solder and a lead-free solder material, Sn–3.5Ag from compression of the specimens using the Shimadzu AG-25 TB Testing Machine, and the Split-Hopkinson Pressure Bar (SHPB) is presented in this section.

Microstructure of Solder Specimens

- **Microstructure of Sn–Pb Solder at Different Cooling Rates**

Distinctly dissimilar microstructures are obtained under different cooling rates. Being polycrystalline structured, the cast solder will develop larger grains at a slower cooling rate (0.1 $°Cs^{-1}$) as grains have more time to nucleate. From Fig. 17, Sn–37Pb solder samples cast from slow cooling (SC) result in larger grains as compared to those formed via moderate cooling (MC) (2–3 $°Cs^{-1}$). Lamellar layers with "lighter-toned" lead and "darker-toned" tin phases are observed for slow-cooled samples. With moderate cooling, the material has less time to resolidify into lamellar layers. As a result, shorter but thicker patches of "light" lead phases suspended in "dark" tin are formed. This is due to the instabilities of advancing liquid–solid interface resulting in island-shaped phases (approximately 5 μm in length) that lack long-range perfection of the lamellar structure formed by slow cooling.

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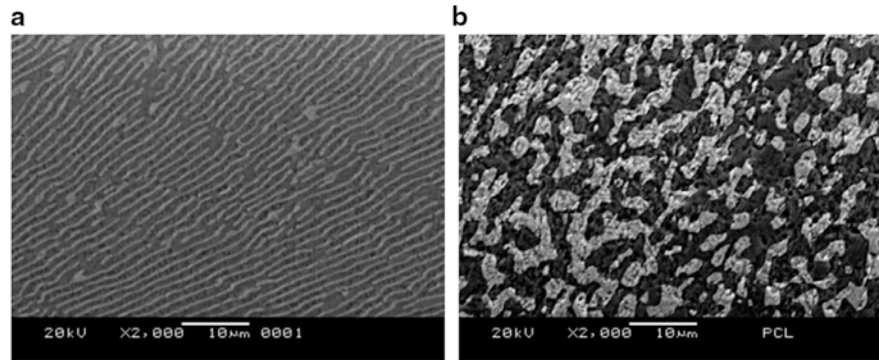

Fig. 17 Representative SEM micrographs of Sn–37Pb formed by (**a**) slow and (**b**) moderate cooling

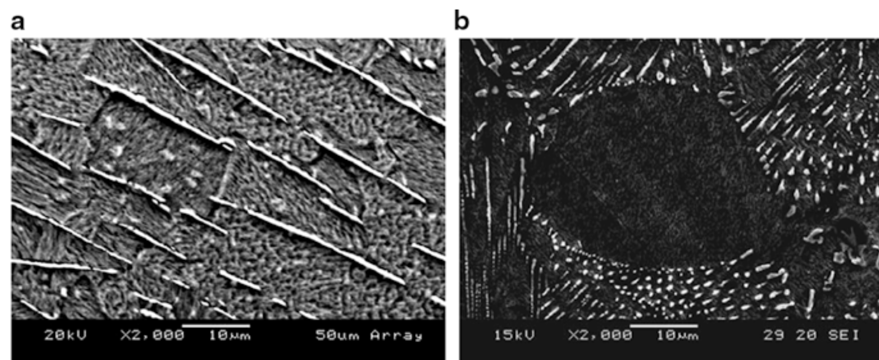

Fig. 18 Representative SEM micrographs of Sn–3.5Ag formed by (**a**) slow (SC) and (**b**) moderate cooling (MC)

- **Microstructure of Sn–3.5Ag Solder at Different Cooling Rates**

Sn–Ag solder, besides having a much higher eutectic temperature of 221 °C, is also very different from Sn–Pb in terms of phase fractions and solubility behavior of the two phases. Lead (Pb) comprises more than 30 % volume fraction in Sn–Pb solder, whereas silver (Ag) comprises less than 4 % of the total volume of Sn-3.5Ag solder and forms mainly the Ag_3Sn intermetallics. (Choi et al. 2000). Also, Pb-rich phases in Sn–Pb solder are ductile as compared to Ag_3Sn intermetallics which are stronger but more brittle (Kim et al. 2002; Maveety et al. 2004). Figure 18 shows slow-cooled (SC) samples produce long, well-aligned Ag_3Sn intermetallic plates/needles. Large Ag_3Sn precipitates are found in the form of platelets/needles, whereas fine Ag_3Sn precipitates are fibrous (Kim et al. 2002). In moderately cooled (MC) samples, Ag_3Sn platelets or needles can be seen to be shorter and less well aligned than in earlier samples formed by slow cooling.

Quasi-Static Compression of Bulk Solders

For quasi-static compression, the bulk solder specimens are prepared by casting and machining methods to produce cylindrical samples approximately 21 mm in length and 7 mm in diameter. The Shimadzu AG-25TB Testing Machine is used to perform the compression tests where specimens were compressed at a strain rate of 8.3×10^{-4} s^{-1} and loaded to 3 % strain (Ong 2005).

Figure 19 shows that Sn–37Pb bulk solder exhibits a slight increase in Young's modulus when cast at higher cooling rates, while this is the reverse for bulk Sn–3.5Ag solder. The Young's modulus for Sn–3.5Ag is about 60 % higher than Sn–37Pb. For the extraction of yield stress, the 0.2 % strain offset method is used to standardize yield stress identification.

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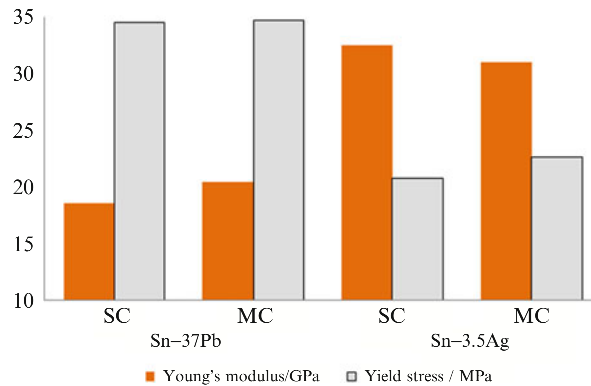

Fig. 19 Young's modulus and yield stresses (0.2 % strain offset) of bulk solders under quasi-static compression

Table 6 Results from high strain rate testing of Sn–37Pb and Sn–3.5Ag solders under dynamic compression

Solder	Cooling	Average yield stress (MPa)	Max flow stress (MPa)
Sn–37Pb	SC (slow cooled)	52	130 at 30 % strain
	MC (moderately cooled)	53	140 at 25 % strain
Sn–3.5Ag	SC (slow cooled)	42	150 at 35 % strain
	MC (moderately cooled)	47	180 at 50 % strain

Dynamic Compression of Bulk Solders

The compressive Split-Hopkinson Pressure Bar (SHPB) experimental setup (Hopkinson 1914) is used to determine the dynamic response of solder specimens under high strain rate compression. The idea of using two Hopkinson bars to measure dynamic properties of materials in compression was developed by Taylor (1946), Volterra (1948), and Kolsky (1949).

The specimens prepared for the Hopkinson bar tests have an aspect ratio of one, and specimen lengths range from 2 to 9 mm. Striker bar velocities ranging from 5 to 15 ms^{-1} were used with the different specimen lengths to attain strain rates ranging from 10^2 to 10^4 s^{-1}.

Table 6 shows the mechanical performance obtained from the dynamic compression of Sn–37Pb and Sn–3.5Ag solders. There is almost no difference in the yield stress of dynamically compressed bulk Sn–37Pb solder for the two rates of cooling. Dynamic results show distinctly higher stresses than quasi-static ones.

Sn–3.5Ag solder, on the other hand, shows an increase in average yield stress and maximum flow stress with faster cooling rate. MC specimens have a maximum flow stress of 180 MPa, while SC specimens only reached a maximum of 150 MPa. Examination of the fractured surfaces showed that there is a transition from ductile to brittle fracture as strain rate is increased.

Tension of Bulk Solders

The transition to lead-free solders is led by the widely adopted Sn–Ag–Cu (SAC) eutectic (Henshall et al. 2008). However, some studies have shown that standard SAC alloys such as SAC 405 (Sn–4 % wt Ag–0.5 %wt Cu) have poorer mechanical performance than eutectic Sn–Pb under high strain rate conditions (Suh et al. 2007).

In this section, bulk solder tensile tests data is presented. The tests are performed by Su et al. (2010) to characterize the mechanical properties of SAC 105 (Sn–1 %wt Ag–0.5 %wt Cu) and SAC 405 (Sn–4 %wt Ag–0.5 %wt Cu) at strain rates ranging from 0.0088 to 57.0 s^{-1}. The bulk

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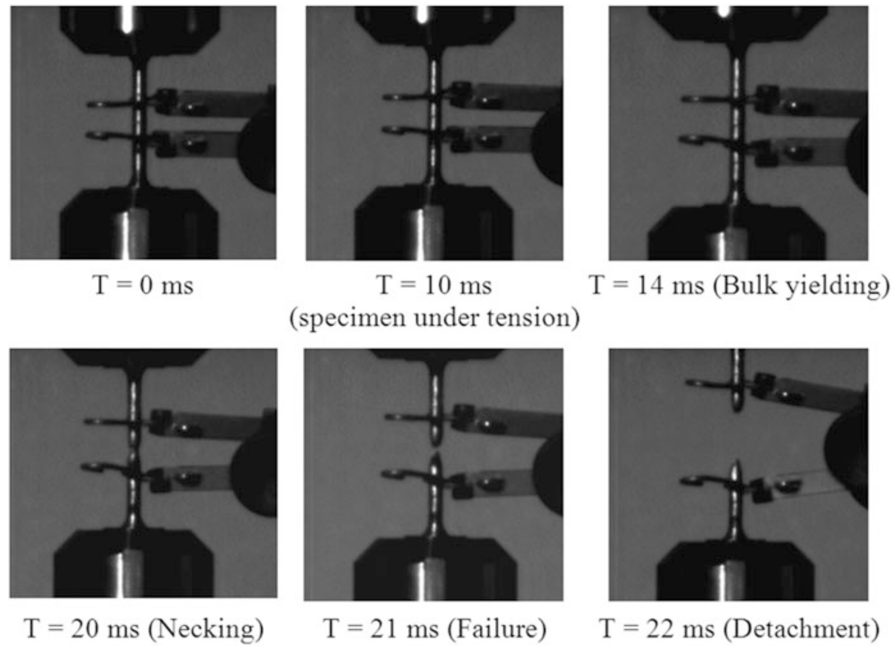

Fig. 20 High-speed camera photography showing dynamic failure of a bulk solder sample

Table 7 Material parameters of rate-dependent yield stress and UTS of different solder alloys

Solder alloys	b_1	b_2	c_1	c_2
SAC 105	40.378	0.0775	53.093	0.0810
SAC 405	48.741	0.0596	67.633	0.0779

solder specimens had a gauge length of 19 mm and diameter of 3 mm as shown earlier in Fig. 15. Results show that Sn–Ag–Cu alloys exhibit higher mechanical strength with increasing strain rate. Furthermore, SAC 105 exhibits about 30 % greater tensile ductility than SAC 405 and Sn–Pb solders. Figure 20 shows a series of high-speed camera pictures depicting the sequence of the test until specimen failure.

(a) **Effect of Strain Rate on Bulk Solder Material Properties**

It is observed that as the rate of loading increases, the strength of the bulk solder material also increases. The trend was similarly observed by both Pang and Xiong (2005) and Che et al. (2008).

For ease of comparison with existing literature, the rate dependence in yield stress and UTS is expressed in the following power relationships:

$$\sigma_y(\dot{\varepsilon})_{Sn-Ag-0.5Cu} = b_1(\dot{\varepsilon})^{b_2} \tag{2}$$

$$\sigma_{UTS}(\dot{\varepsilon})_{Sn-Ag-0.5Cu} = c_1(\dot{\varepsilon})^{c_2} \tag{3}$$

The coefficients b_1, b_2, c_1, and c_2 are listed in Table 7.

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The coefficients *b* and *c* directly relate to the strain rate sensitivity of yield stress and UTS respectively. Strain rate sensitivity can be useful in the study of the ductile to brittle transition strain rate (DTBTSR) in solder joints, which is affected by the sensitivity of bulk solder strength to strain rate.

(b) **Effect of Ag Content on Mechanical Properties of Bulk Solder**

The yield stress and UTS of SAC 405 are consistently higher than SAC 105, while elongation decreases with higher Ag content for lead-free alloys. The trend is similarly reported by Che et al. (2008). Sn–Ag–Cu alloys are strengthened by the internal stress accumulated due to the difference in elastic modulus and volume fraction between Ag_3Sn and Sn matrix (Reid et al. 2008). Higher Ag content will increase the amount of Ag_3Sn phase (Darveaux and Reichman 2006), contributing to the higher strength of SAC 405 (Suh et al. 2007).

(c) **Failure Analysis of Fractured Dog Bone-Shaped Bulk Solder Test Specimens**

Figure 21 shows the fractured solder specimens after test. 45° shearing is the primary mode of failure at lower strain rates, while necking is mostly observed at higher strain rates.

The study conducted by Su et al. (2010), concluded that solder alloy materials such as SAC 105 and SAC 405 exhibited higher mechanical strength (in terms of yield stress and UTS) with increasing strain rate as compared to that of traditional Sn–Pb solders. Furthermore, rate-dependent properties such as mechanical strength exhibited linear relationship with respect to strain rate expressed in power scale. For the Sn–Ag–Cu alloys, the bulk solder material properties such as strength and ductility are also observed to vary with different Ag content.

Mechanical Study of Solder Joints

Mechanical reliability has become an issue (Frear et al. 1999) as electronic components and solder joint dimensions shrink. Solder joints are expected to undergo high strain rate conditions especially for products developed for use in shock loading environments in the automotive, aerospace (Darveaux and Reichman 2006), marine and offshore, and portable consumer sectors. The industry has also made a transition towards the adoption of lead-free solder alloys, commonly based around the Sn–Ag–Cu formulations (Henshall et al. 2008).

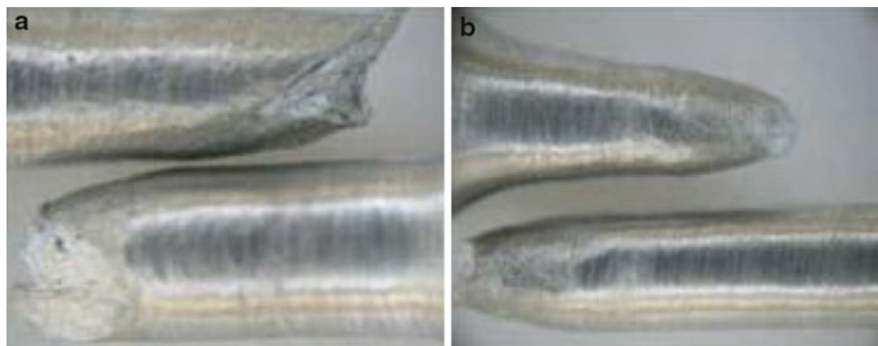

Fig. 21 Photographs of fractured dog bone-shaped bulk solder tensile test specimens. (**a**) Test rate of 10 mm/min, showing 45° shear failure mode, (**b**) test rate of 22,500 mm/min, showing necking failure mode (Su et al. 2010)

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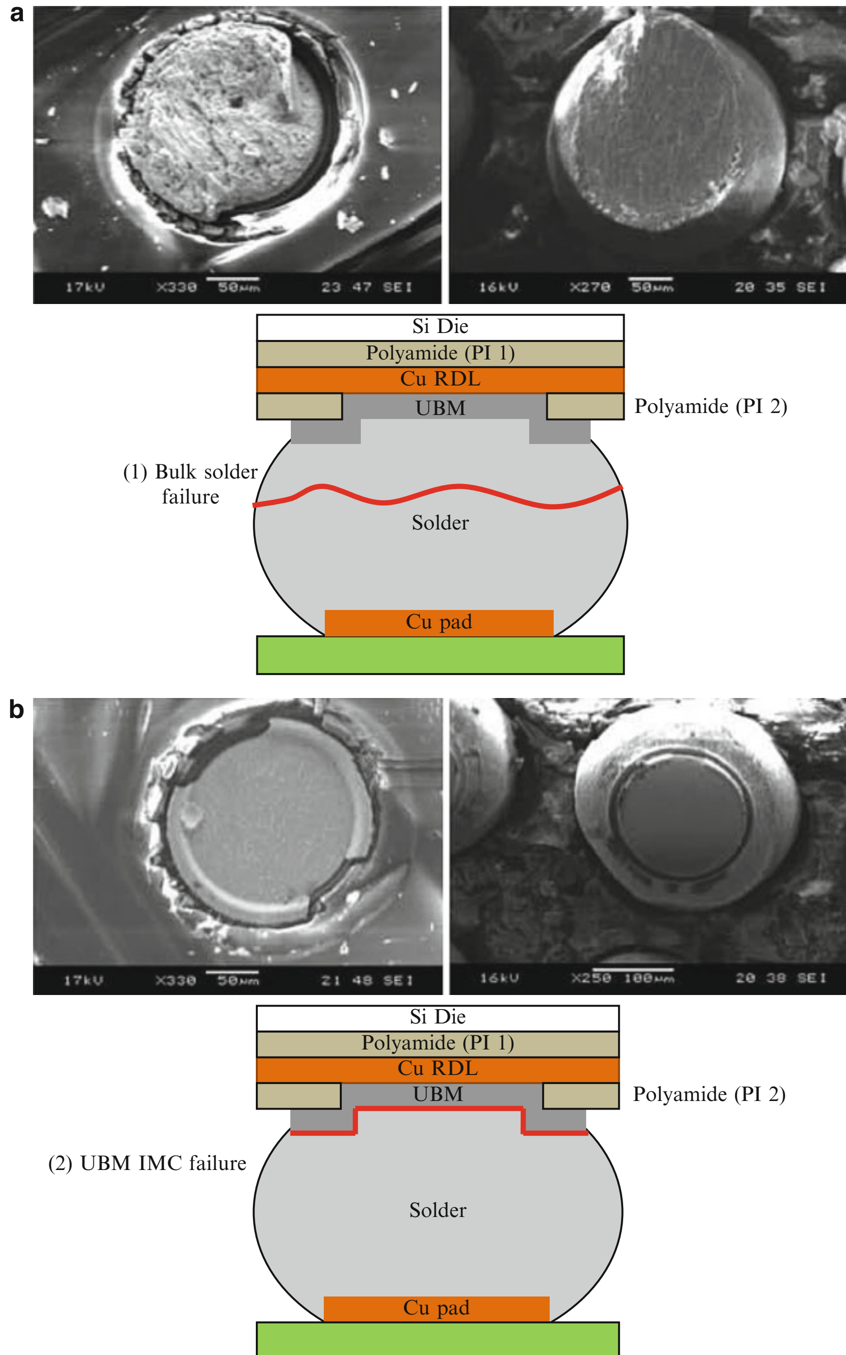

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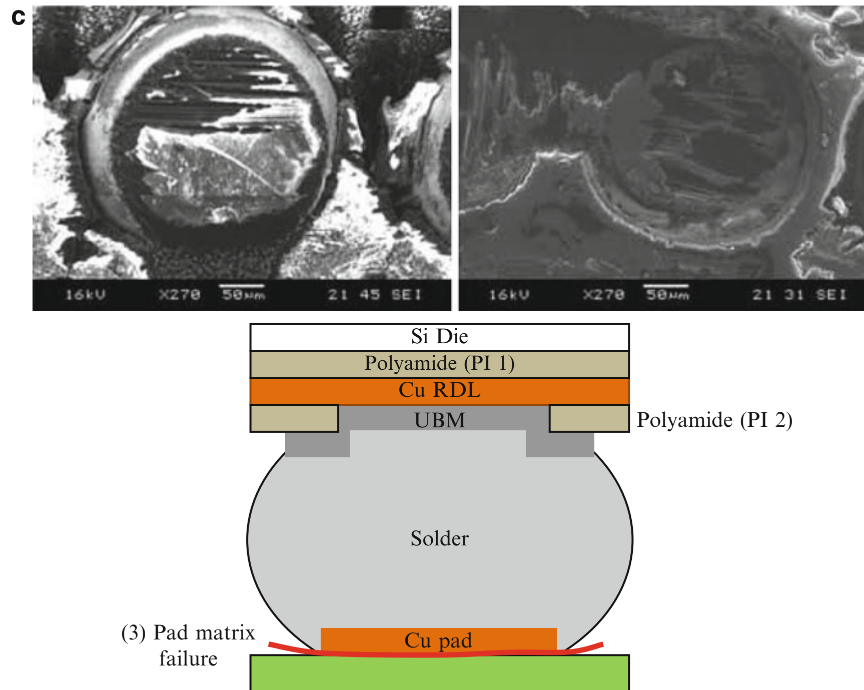

Fig. 22 Schematic diagrams and fractographs showing (**a**) bulk solder failure, (**b**) UBM–IMC failure, and (**c**) pad matrix failure on solder joints (Extracted from (Su et al. 2010))

In this section, the results of package pull and shear tests conducted by Su et al. (2010) are presented to illustrate the effects of strain rate, silver content in Sn–Ag–Cu solder joints, and loading orientation on the reliability of the microelectronic packages.

Wafer-level chip scale packages (WLCSP) with SAC 105 or SAC 405 alloy solder joints are test under room conditions, at 0.5 mm/s (2.27 s^{-1}) and 5 mm/s (22.73 s^{-1}). Each WLCSP specimen has an array of 12 by 12 solder joints sandwiched between a die substrate and a printed circuit board. These WLCSP have solder bumps that are 300 µm in diameter and double redistribution layers with a Ti/Cu/Ni/Au under bump metallization (UBM) as their silicon-based interface structure.

Results of Solder Joint Array Shear and Tensile Tests

Solder joints that were fractured during tests were examined to determine their modes of failure. Both Darveaux et al. (2006) and Zhao et al. (2007) have identified three major modes of solder joint failures for ball grid array packages (BGAs), namely, (i) ductile bulk solder failure, (ii) brittle interface fracture at the intermetallic compound (IMC) layer, and (iii) pad matrix failure. Figure 22 shows the typical failure modes accompanied by cross-sectional schematics to show the location of each failure.

(a) **Bulk solder failure**. Bulk solder failure occurs by fracturing through the solder sphere and is usually detected near the die side interface and can be easily identified by the silvery solder residue on the entire pad of the die substrate. The failure surface is usually undulating and less smooth than those seen for the UBM-IMC failures.
(b) **UBM –IMC failure**. The failure crack usually occurs in the intermetallic compounds (IMC) which are usually more brittle than the bulk solder (Frear et al. 1999) or at the interfaces with the substrate. It can be identified by a smooth surface on the die substrate or a characteristic ring step and smooth surface at the top of the solder bump.

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(c) **Pad matrix failure**. Pad matrix failure occurs across the matrix layer of the fiber-epoxy polymer composite that makes up the printed substrate or board. It can be identified by "cratering" (Henshall et al. 2008) in the board side.

Bulk solder failure is commonly regarded as a desirable mode of failure to avoid catastrophic failures (Darveaux et al. 2006). Wong et al. noted that bulk solder failures correspond to high drop test life of ball grid array packages (BGAs), which is more desirable than IMC failures that correspond to low drop test life (Wong et al. 2008a).

Derivation of Average Solder Joint Array Strength From the load–displacement raw data, the average stress in the solder joint array can be calculated by dividing load over the sum of joint pad area (Darveaux and Reichman 2006). The total failure cross-sectional area (A_T) can be obtained as follows:

$$A_T = \sum_i A_i = \sum_i a_i n_i \tag{4}$$

where $i = 1$ corresponds to failure mode 1 (e.g., bulk solder failure), $i = 2$ corresponds to failure mode 2 (e.g., UBM–IMC failure), etc. a_i is the cross-sectional area of the failure region in a single solder bump. The number of solder joints that failed under each mode (n_i) is determined from the optical images of the fractured solder joint array sample after testing.

The average solder joint array strength (σ_{ave}) is calculated by dividing peak load (F_{max}) over the total failure cross-sectional area, A_T:

$$\sigma_{ave} = \frac{F_{max}}{A_T} \tag{5}$$

Solder joint strength refers to the strength of the entire solder joint that consists of a multitude of different materials making up the joint, and thus, the failure of the solder joint may not lie within a particular material, but at the interfaces (UBM/RDL or solder/IMC). Table 8 lists the solder joint array test results of SAC 105 and SAC 405 alloys.

Table 8 Tensile and shear test results of SAC 105 and SAC 405 solder joint arrays (Data extracted from (Su et al. 2010))

			Failure mode count, n_i			
Solder material	Loading orientation	Test rate (mm/s)	Bulk solder	UMB IMC	Cu RDL	Pad matrix
SAC 105	**Tension**	**5**	0	5	1	139
		0.5	0	33	1	111
	Shear	**5**	0	64	4	77
		0.5	75	0	0	70
SAC 405	**Tension**	**5**	0	0	0	144
		0.5	0	6	0	139
	Shear	**5**	0	108	3	33
		0.5	35	1	0	107

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Effect of Strain Rate

(a) Ductile to Brittle Transition

Sn–Ag–Cu solder alloys generally attain higher strength at higher strain rates (Pang and Xiong 2005; Che et al. 2008). As the test rate increases, the solder in the joints become stronger and more resistant to mechanical loading and the applied loading stress will increasingly accumulate at the solder joint interfaces (Darveaux et al. 2006) due to their proximity to geometric discontinuities leading to brittle interface failures. Darveaux had investigated the ductile to brittle transition strain rate (DTBTSR) by performing solder joint array tensile tests (Darveaux and Reichman 2006). The ductile to brittle transition strain rate (DTBTSR) is defined as the strain rate at which 50 % of the joints fail at the pad interface (Darveaux and Reichman 2006). In this study, "ductile to brittle transition strain rate" will simply be the strain rate where 50 % of the joints fail at the bulk solder. "Interfacial failure" will collectively refer to all the other non-bulk solder modes of failure.

(b) Effect of Strain Rate on Solder Joint Array Strength

Figure 23 shows the average solder joint array strength of the tested specimens (SAC 105 and SAC 405 alloys) at two different test rates (0.5 and 5.0 mm/s) under shear and tension. It is observed that the average solder joint array strength decreases at higher strain rates, regardless of solder alloy material and test orientation. Newman (2005) and Darveaux et al. (2006) had previously observed higher strength at higher shear rates in solder ball impact shear tests. However, Darveaux et al. also noted that solder joint strength declined at even higher strain rates when "interface failures start to occur" (Darveaux et al. 2006).

(c) Effect of Strain Rate on Failure Mode (Under Shear)

Figure 24 shows the percentage distribution of failure modes observed under shear tests. It is observed that there is a decrease in bulk solder failures to eventually no such failure at higher strain rates (Darveaux and Reichman 2006). UBM–IMC failure is prominent at higher shear application rates due to the transition from ductile (cohesive) to brittle (interface) failures. Pad matrix failure is observed to be increasingly dominant for SAC 105 as the strain rates increase for shear. In contrast, SAC 405 has a reduction of pad matrix failures but an increase of UBM–IMC failures at the higher strain rate. The observed failure modes transition may be a result of the

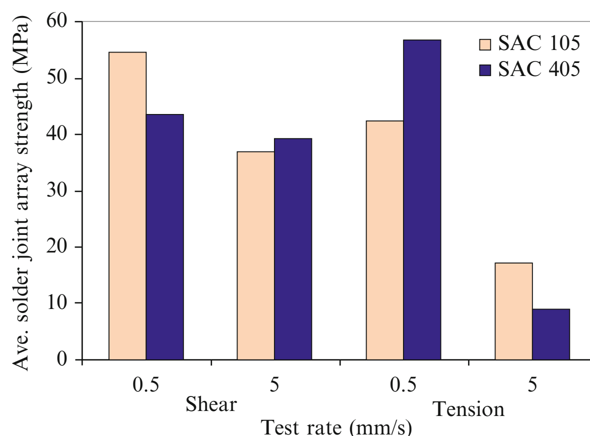

Fig. 23 Solder joint array strength of SAC 105 and SAC 405 solder alloys at different test rates under shear and tension (Data from (Su et al. 2010))

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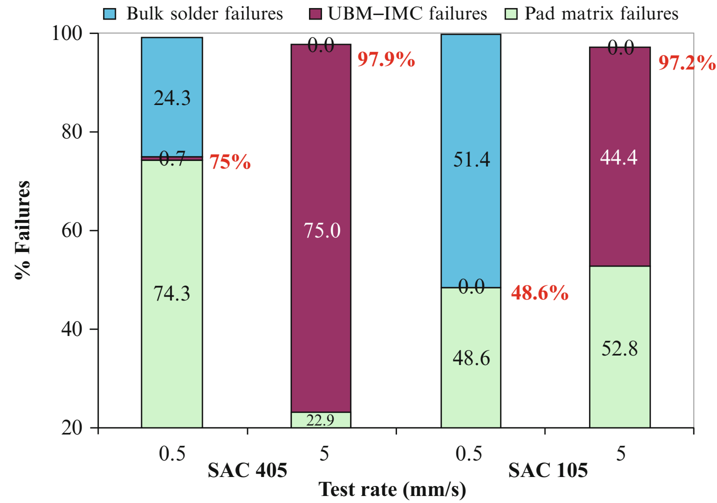

Fig. 24 Graphical illustration showing the different failure mode % against test rate under shear (Data from (Su et al. 2010))

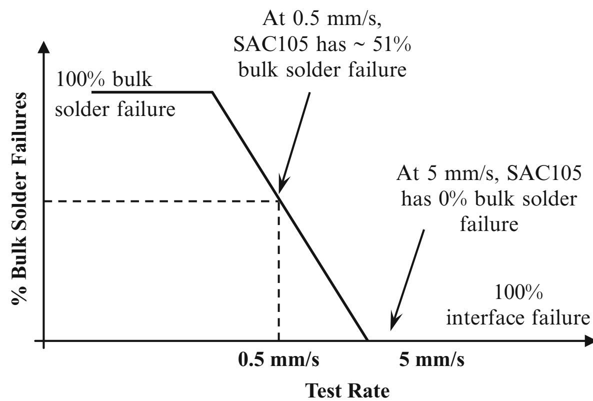

Fig. 25 Experimental result of SAC 105 superimposed onto the ductile to brittle transition strain rate model under shear (Adapted from (Su et al. 2010))

UBM–IMC layer being weaker than pad matrix layer at the higher test rate. Figure 25 shows the experimental results of SAC 105 superimposed onto the ductile to brittle transition strain rate (DTBTSR) model, under shear.

(d) **Effect of Strain Rate on Failure Mode (Under Tension)**

Figure 26 shows the experimental results of SAC 105 superimposed onto the DTBTSR model under tension. No bulk solder failure is observed for the two test rates which are in contrast to the results obtained from shear. As no bulk solder failure is observed under tension, the competing failure is between the various interfacial regions such as the UBM–IMC and pad matrix. It was observed that there is generally more pad matrix failures at the higher test rate of 5 mm/s, which results in correspondingly less UBM–IMC failures. The percentage of pad matrix failures increased to almost 100 % at 5 mm/s.

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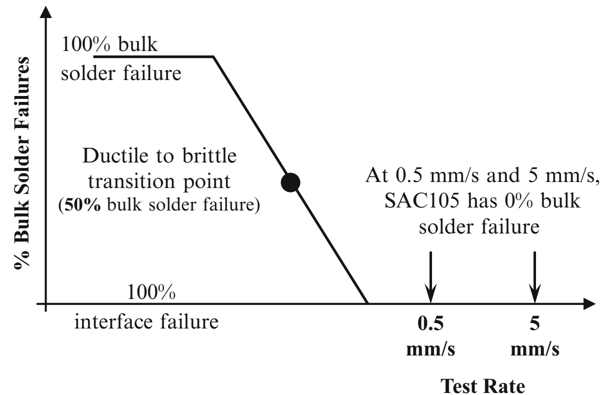

Fig. 26 Experimental result of SAC 105 superimposed onto the ductile to brittle transition strain rate model under tension (Adapted from (Su et al. 2010))

(e) **Effect of Ag Content on Failure Mode**

SAC 105 experiences more bulk solder failures than SAC 405 under 0.5 mm/s shear speed. It is expected that higher Ag content will result in higher bulk alloy strength under the same test speed; therefore, SAC 105 (1 % Ag) joints are seen to obtain lower strength than SAC 405 (4 % Ag) at 0.5 mm/s. For 5 mm/s, the trend is contrary as the higher rate has already caused the increase in interface failures for SAC 405 that resulted in a decline in overall joint strength. SAC 405 bulk solder is more load resistant, thereby transferring more loading stress to the interfaces, resulting in more interface failures than in SAC 105 solder joints. Kim et al. conducted drop tests and found that IMC cracking at the package side was predominant in SAC 405, while SAC 105 had more bulk solder failures (Kim et al. 2007).

(f) **Effect of Ag Content on Solder Joint Array Strength**

At higher test rates, solder joint arrays with lower Ag content are better able to withstand higher loads before failure occurs. Therefore, solder joints with Sn–Ag–Cu alloys of low Ag content are seen to improve the mechanical reliability of microelectronic packages under high strain rate conditions by reducing stress localizations to material interfaces than would a higher rate-sensitive solder like SAC 405.

(g) **Effect of Loading Orientation**

Specimens under tension generally have lower ductile to brittle transition strain rate (DTBTSR) than specimens under shear (Zhao et al. 2000). From the results of the solder joint array tests, Su et al. (2010) concluded that the average solder joint array strength decreased at higher strain rates. It was observed that for similar alloys, more interface failures were observed at higher strain rate. High Ag content Sn–Ag–Cu joints generally yielded more interface failures and lower peak loads than those with lower Ag content. Furthermore, solder joints under shear loading were found to produce more bulk solder failures and higher average solder joint strength, peak load, and ductility than those under tensile loading.

Mechanical Study of Single Solder Joints

Solder joint strength testing such as ball shearing (Wang et al. 2003), package peel test (Wang et al. 2003; Bragg et al. 2003), and board bending (Lau 1996) while useful has certain inherent limitations. Ball shear tests, for example, may show wrong failure initiation modes. Similarly, drop

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impact samples may show solder bulk failure (Wang et al. 2003) instead of either pad peel offs or intermetallic failure at the solder/pad interfaces which are the usually observed failure modes. In this section, the work of Tan et al. (2009) on the testing and failure analyses of single solder joints under combined normal and shear loads is presented.

Micromachining is performed on "as-reflowed" printed circuit board (PCB) assemblies to produce the single-joint samples. Figure 27a illustrates the schematics and dimensions of the fixtures used, and Fig. 27b shows an example of the end product after the single-joint specimen is bonded to the fixtures. All joints are tested at the rate of 100 μm/min. Loctite™ 4105 kit instant adhesive (cyanoacrylate) is used to bond the samples to the fixtures. The samples are then tested on a micro-Instron tester.

(a) **Tension/Shear Test Results**

As the loading changes from pure tension to mixed tension/shear and then to pure shear for the different batches of test, the joint failure forces decreases. For most tests concerning 0° and 30° loading directions, rapid degradation of force correlated to pad peel off can be observed, while 60° and 90° tests displayed gradual force reduction often revealing solder yield failure in posttest analysis.

(b) **Compression/Shear Test Results**

The average results for the various sets of single solder joint tests showed that the joint failure forces are the highest for pure tension and pure compression under the test rate of 100 μm/min.

(c) **Failure Mapping and Criterion Formulation**

Using the results acquired, a mapping of the joint failure forces such as Fig. 28, in terms of tension, shear, and compression components, can be plotted.

The empirical expression of the failure criterion is as follows:

$$\frac{(F_T - a)^2}{b^2} + \frac{(F_s)}{c^2} \leq 1 \tag{6}$$

where a, b, and c are the constants defining the vertical shift of the plot, the averaged value for pure tension/compression failure (performed at 0° and 180°), and the value for pure shear (performed at 90°). This failure map allows component and system manufacturers to design packages and to determine their layout locations against overload type of loading environment.

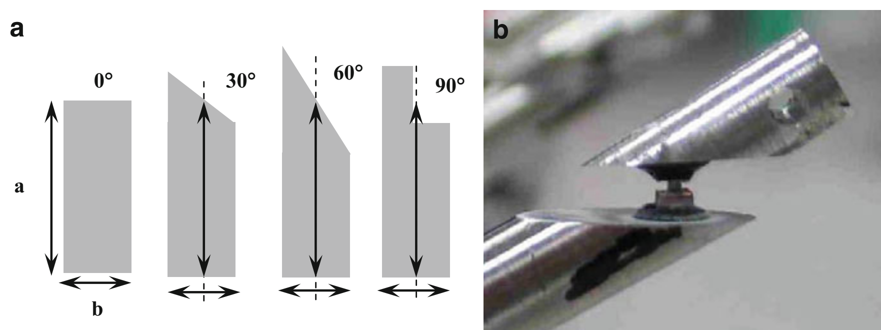

Fig. 27 (**a**) Schematic diagrams of 4 types of fixture (0°, 30°, 60°, 90°) bonded to single-joint specimens. (**b**) Photo showing a sample bonded on a 60° fixture (Adapted from (Tan et al. 2009))

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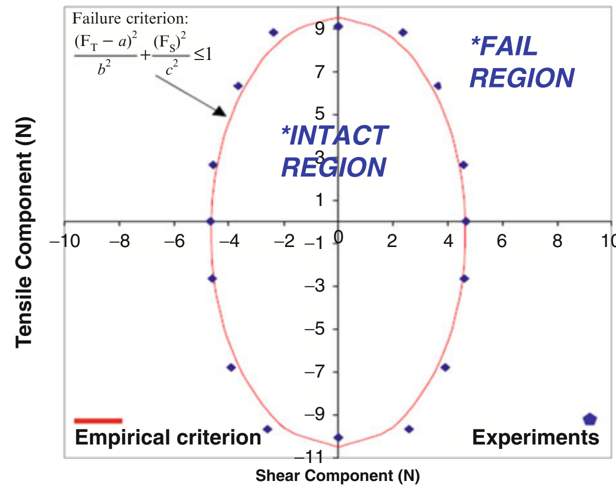

Fig. 28 Failure mapping and criterion formulation (Extracted from (Tan et al. 2009))

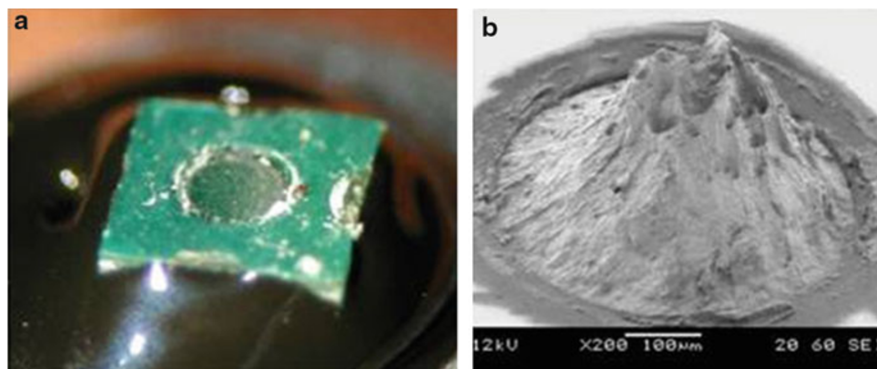

Fig. 29 (**a**) Photo showing PCB pad peel off and (**b**) fractograph showing hillock, after subjected to 0° pure tension (Extracted from (Tan et al. 2009))

(d) **Failure Analysis of Tested Joints**

0° Pure Tension: Specimens under tension show either gross bulk yielding which gradually leads to joint failure or pad peel off that is catastrophic and sudden (Fig. 29). Energy dispersive spectroscopy (EDX) did not reveal any presence of intermetallics on the failure surfaces of the specimens subjected to tensile loading.

30° Tension/Shear: SEM inspection of the failed specimens (Fig. 30) for this loading condition showed that almost all joints fail by bulk yielding near the substrate interface, whereby the hillock is characteristically at the leading/trailing edge of the pad in the direction of shear. EDX performed on the failure surfaces revealed fracture occurring at the bulk solder, and no failure at the intermetallic is found.

60° Tension/Shear: The nonuniformity of stress distribution via the application of 60° tension/shear load causes much localized stresses at the pad edges, which then causes the joint to fail at substrate interfaces rather than the solder bulk. Some failed surfaces (Fig. 31) show failure across the solder/metallic pad layer, implying that the fracture surface no longer lies purely at the bulk solder region.

90° Shear: The dominant failure mode for this loading condition is bulk solder failure which occurs at very close to the pad interfaces, and no pad peel off is observed.

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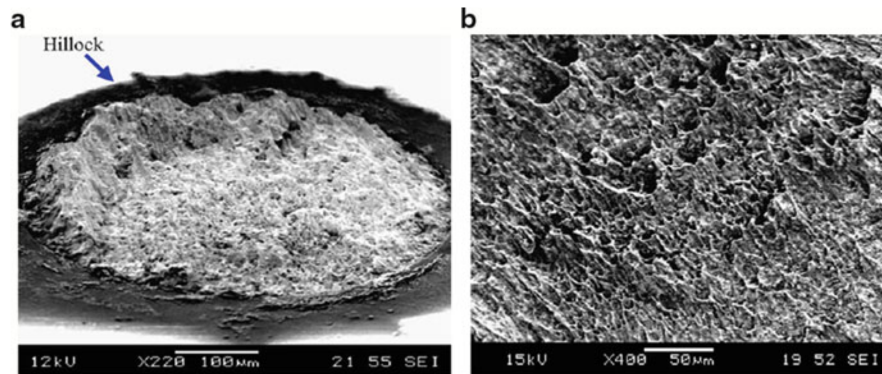

Fig. 30 Fractographs showing (**a**) an incline view and (**b**) a close-up view of the fractured surface, after subjected to 30° tension/shear (Extracted from ref. (Tan et al. 2009))

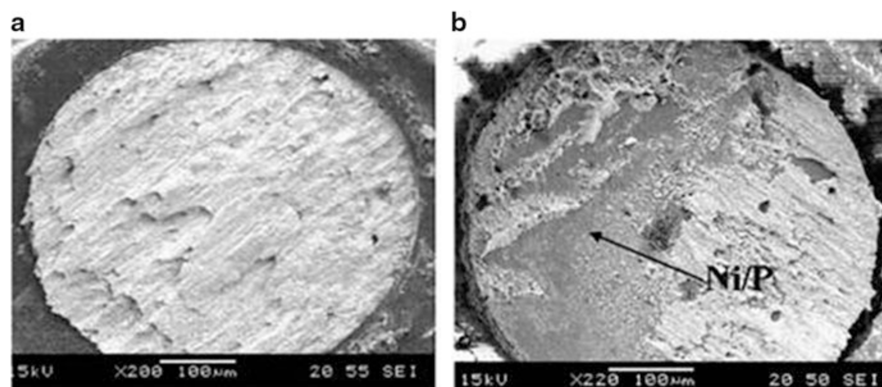

Fig. 31 (**a**) Fractograph showing a "smooth" failure surface and (**b**) EDX elemental analysis of the fractured surface, after 60° tension/shear (Extracted from ref. (Tan et al. 2009))

60° and 30° Compression/Shear and 0° Compression: Optical inspection of the failed specimens shows that almost all failures due to compression/shear occur at the substrate/solder interface. For 30° and 0° compression loading, the specimens do not readily produce a failure surface since the stress states are predominantly compressive. General observations show global gross shearing and compression of the solder joint. Since for compression tests, only the yield strength of the joint is needed to generate the failure map, tests were stopped when yield is obvious.

From the study conducted by Tan et al. (2009), the researchers have demonstrated that the failure mapping and modes obtained from single-joint tests are able to predict board-level joint failure well. This illustrates the independent nature of the failure mapping methodology in effectively predicting board failures due to combined loading on various board geometries with different boundary conditions.

Temperature Cycling Reliability

When an electronic package is in service, the solder joints are subjected to a wide range of temperatures as a result of the device being powered on and off. As a result, these solder joints often fail under cyclic thermal loading as they accommodate the difference in thermal expansion

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(CTE) of electronic materials within the assembly. Therefore, in order to predict the reliability of solder joints under service condition, it is of paramount importance to investigate the reliability issues of solder joints under temperature cycling condition.

Temperature Cycling Test Conditions

During the temperature cycling test, the test samples are placed into test chambers and are subjected to alternating temperature extremes. It is carried out with the aim to test the mechanical reliability of the joints. This is done by designing a test vehicle containing daisy chains to form a circuit of typical electrical resistance 0.5–1.5 Ω. The repeated cycling at high and low temperatures subjects the joints to fatigue, resulting in crack initiation and propagation in the joints. This causes an increase in electrical resistance of the daisy chains in the sample. Both C4 and BGA solder joints can be tested in this test. C4 joints are tested in a component level test, where the components are not mounted onto PCBs. Large CTE mismatch between the die (2.6×10^{-6}/K) and substrate (20×10^{-6}/K to 25×10^{-6}/K) results in large shear stresses in C4 joints. This can lead to fatigue failure. Underfill is often used to improve the reliability of these joints. To test solder joints, components are reflowed onto a PCB and the level two daisy chains are monitored instead of level one joints. Several test temperature conditions have been recommended (JEDEC Solid State Technology Association 2005), and these are presented in Table 9. In electronic packaging of consumer products, test conditions G and J are more commonly used.

Evaluation Study on Five Pad Finishings Using Temperature Cycling Test

Temperature cycling test was carried out on packages with five different pad finishings to evaluate their temperature cycling reliability. The substrate pad finishes evaluated were (i) electrolytic nickel–gold (NiAu), (ii) organic solderability preservative (OSP), (iii) stencil printed solder-on-pad (SoP), (iv) immersion tin (ImSn), and (v) electroless nickel–electroless palladium–immersion gold (NiPdAu). The loading profile used ranged from −40 °C to 125 °C with ramp and dwell times of 15 min each. PCB thickness used was 1.1 mm.

The number of cycles to failure of each package in each leg was fitted to a two-parameter Weibull distribution. The Weibull distribution is commonly used to determine mean life of parts for cases

Table 9 Various temperature cycling test conditions and cycling temperatures (JEDEC Solid State Technology Association 2005)

Test condition	Cycling temperatures	
	T_{min} (°C)	T_{max} (°C)
A	−55	85
B	−55	125
C	−65	150
G	**−40**	**125**
H	−55	150
I	−40	115
J	**0**	**100**
K	0	125
L	−55	110
M	−40	150
N	−40	85

Test conditions shown in bold are more commonly used in for consumer microelectronics products

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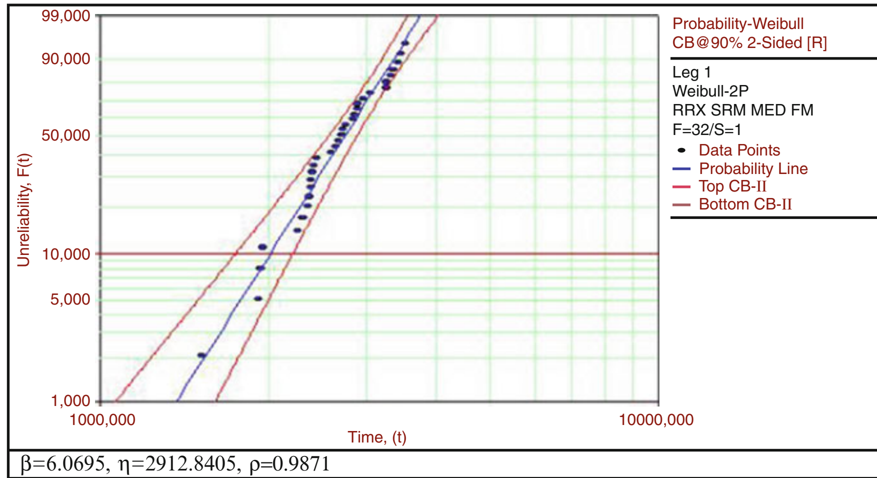

Fig. 32 Representative Weibull plot showing temperature cycling data from NiAu finishing sample (Extracted from (Wei et al. 2008))

Table 10 Weibull parameters for the various legs of temperature cycling test (Extracted from (Wei et al. 2008))

			Weibull parameters	
Leg	Pad finishing	Package size/no. of balls (mm^2/60)	η	β
1	NiAu	11 × 10.5	2912.8	6.070
2	OSP	11 × 10.5	1125.0	6.188
3	SoP	11 × 10.5	2283.2	10.488
4	ImSn	11 × 10.5	2287.2	10.081
5	NiPdAu	11 × 10.5	2266.6	6.734

where failure occurs as a result of wear-out such as solder joints. The two-parameter Weibull probability distribution function (PDF) is

$$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} e^{-\left(\frac{t}{\eta}\right)^{\beta}} \tag{7}$$

where *f(t)* is the PDF, β the shape parameter, η the characteristic life, and t the time.

A representative Weibull plot is shown in Fig. 32 for NiAu. The Weibull parameters (β and η) were then extracted and are shown in Table 10. From η in Table 10, it is clear that NiAu performs the best under TC and OSP the worst. Cross-sectional analysis is also performed on failed parts to determine the location of failure. A representative cross section of solder joint is shown in Fig. 33 where there is a through crack at the top of the joint (Wei et al. 2008).

Simulation

Finite element analysis (FEA) of temperature cycling is carried out for the purpose of life prediction for BGA solder joint. Typically, commercial FEA software such as ANSYS™ or Abaqus™ is used. The general methodology used in carrying out such an analysis is outlined here.

- **Step 1: Creating the FEA model**

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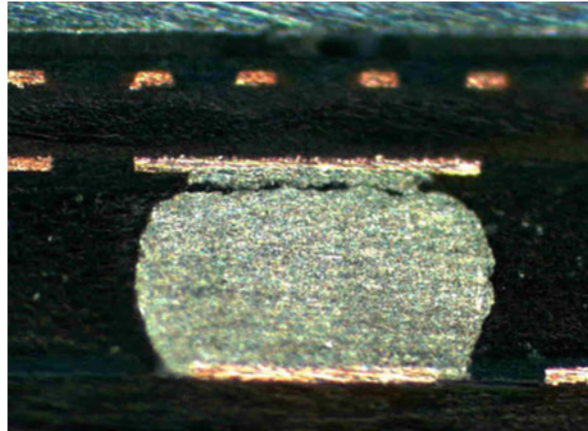

Fig. 33 Through crack in bulk solder at the top of the solder joint (Extracted from (Wei et al. 2008))

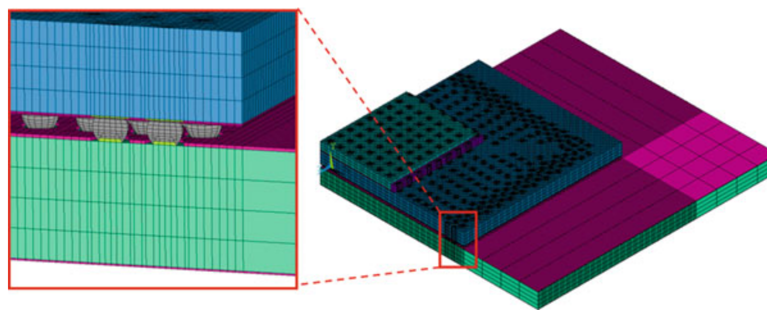

Fig. 34 Quarter FEA model of electronic package

A CAD model of the package to be analyzed is usually created and meshed. As a rectangular electronic package has two planes of symmetry, a quarter model of the package is typically used. Depending on the computational power available, a one-eighth model or diagonal slice model may be used for life prediction. Typical quarter finite element model used in electronic packaging is shown in Fig. 34.

The details of the solder joints are modeled accurately – especially the dimensions of the solder resist opening (SRO) and whether the pad is solder mask defined (SMD) or non-solder mask defined (NSMD). Figure 35 shows the details of a pad structure of a BGA joint. Failure in temperature cycling occurs near the pad (as shown in Fig. 33), and an accurate representation of this region will produce better simulation data.

- **Step 2: Defining Material Properties**

  Rate-dependent viscoplastic properties must be defined for the solder alloy in the model. The Anand model with nine material properties is commonly adopted. In this model, creep is described by the following flow equation (Chang et al. 2006; Darveaux et al. 1995):

$$\dot{\varepsilon}_p = A\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}} exp\frac{-Q}{RT} \tag{8}$$

where $\dot{\varepsilon}_p$ is the inelastic strain rate, A is an empirical constant, Q is the activation energy, R is the gas constant, ξ is the stress multiplier, σ is the equivalent stress, s is the internal state variable, and m is the strain rate sensitivity parameter.

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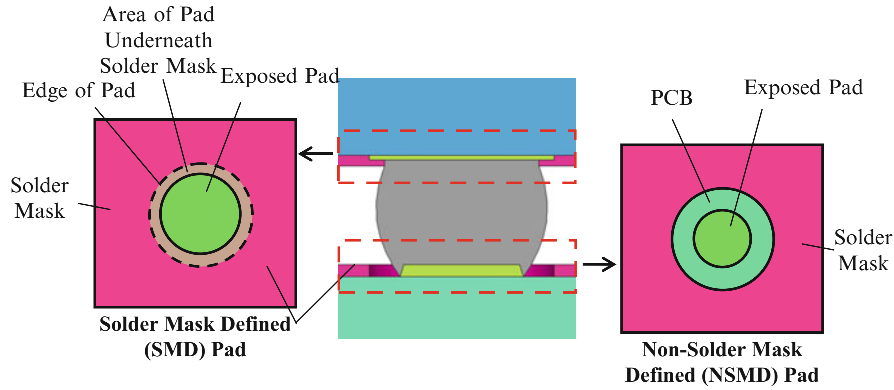

Fig. 35 Details of a pad structure of a BGA joint

The evolution equation is given by

$$\dot{s} = \left\{ h_0 (|B|)^a \frac{B}{|B|} \right\} \frac{d\varepsilon_p}{dt} \tag{9}$$

where

$$B = 1 - \frac{s}{s^*} \tag{10}$$

and

$$s^* = \hat{s} \left\{ \frac{1}{A} \frac{d\varepsilon_p}{dt} \exp\left(\frac{Q}{RT} \right) \right\}^n \tag{11}$$

where h_o is the hardening/softening constant, a is the hardening/softening strain rate sensitivity coefficient, s^* is the saturation value of s for a given set of temperature and strain rate data, $\hat{s}$ is the saturation coefficient, and n is the strain rate sensitivity coefficient for the saturation value of deformation resistance. The Anand constants for Sn–Pb and SAC 305 are given in Table 11.

In addition to the properties of the solder joint, the orthotropic properties of the board and substrate, as well as the CTE values, need to the measured and input into the model.

- **Step 3: Defining Loading Conditions**

  The model is then subjected to three temperature cycles as shown in Fig. 36. Symmetry boundary conditions are specified along the cut boundaries of the symmetric models.

- **Step 4: Analyzing the Results**

  Once the computer simulation has completed running, the results can be analyzed. Typically the Mises stress contour and the creep strain energy density contours (shown in Fig. 37) are used to determine the location of the joint with the highest damage.

Table 11 Anand constants for Sn–Pb and SAC 305 solder alloys (Extracted from (Schubert et al. 2003; Darveaux 2000))

Solder alloy	s_0 (MPa)	Q/R (K)	A(s^{-1})	ξ	m	h_o (MPa)	$\hat{s}$ (MPa)	n	a
Sn–Pb	12.4	9,400	4e6	1.5	0.303	1,379	13.8	0.07	1.3
SAC 305	45.9	7,460	5.87e6	2	0.0942	9,350	58.3	0.015	1.5

s_0 is the initial value of s, used to compute B in Eq. (10)

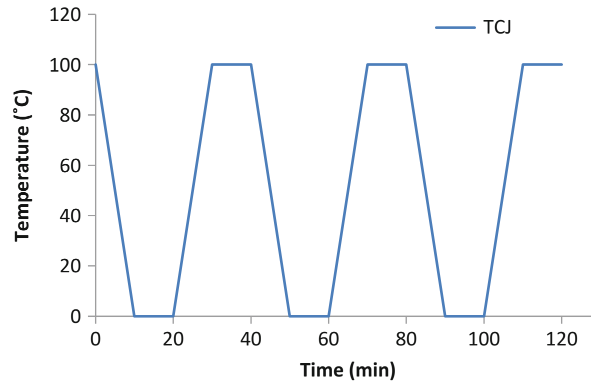

Fig. 36 Loading condition of three temperature cycles which is applied on the model

For the purpose of life prediction, the creep strain energy density (ΔW) in the third cycle is used as the reference stress. ΔW is given by

$$\Delta W = \frac{\sum_{i=1}^{n} (\Delta w_i \times V_i)}{\sum_{i=1}^{n} V_i} \tag{12}$$

where Δw_i is the change in creep strain energy density for element i in the region of interest, V_i the volume of element i, and n the number of elements in the region of interest. Δw_i and V_i are extracted from the software for all elements in the region of interest. The ΔW can then be computed using Eq. 12.

Volumetric average of creep strain energy is used to reduce the effect of singularities at joint corners. The region of interest was defined as the neck of the solder joint as shown in Fig. 38. Typically it may consists of one or two layers of elements at the top of each joint.

- **Step 5: Correlation with Experimental Results**

  The energy density-based life prediction model based on the power law is typically used and is shown below (Anand 1985):

$$N_f = (C\Delta W)^{-n} \tag{13}$$

where N_f is the number of cycles to failure, C is a constant, n is an exponent that is close to 1 (Syed et al. 2008, 2007), and ΔW is the creep strain energy density accumulated per cycle.

  Correlation with experiments is carried out by plotting number of cycles to failure against ΔW. This plot is then fitted to Eq. 13 so that the constants C and n may be determined. Determining the constants based on a larger data set will give the model greater confidence. Note that C and n will vary with solder alloy, pad finishing, and package type.

- **Step 6: Life Prediction**

  Once the constants C and n in Eq. 13 are determined, life prediction can be carried out. FEA models need to be created for the packages in question and the ΔW extracted from the models. Using Eq. 13 and the constants determined in Step 5, BGA joint life may be calculated.

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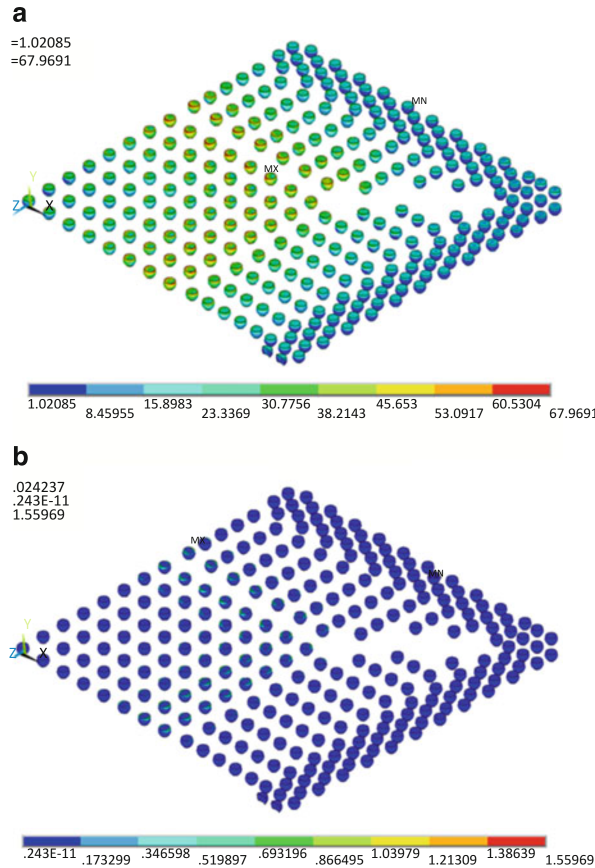

Fig. 37 (**a**) Mises stress contour and (**b**) creep strain energy density on solder joints

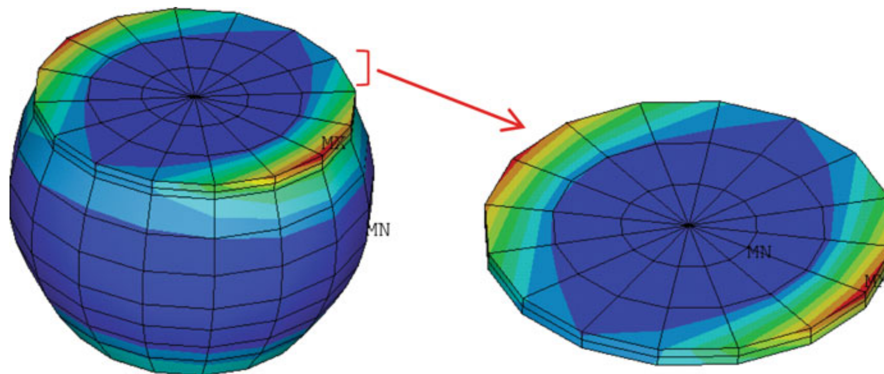

Fig. 38 Creep strain energy density contour on a single solder joint and region of interest used to determine volume-averaged ΔW

Drop Impact Reliability

With the advancement of technology in consumer products and the increase in popularity of portable electronic items like laptops and mobile phones, the failure of solder joints through accidental drop impact has increasingly become a concern. In an effort to minimize this failure, product-level drop impact testing is actively being carried out by the manufacturers of such products. In addition to product-level drop testing which simulates field conditions better as a result of the orientation of

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impact, board-level drop test is also carried out. Product-level tests are more difficult to analyze as during some drops, the product might bounce and this would result in multiple impacts on the product. Furthermore, conducting such testing only at the end of the entire assembly chain will be a costly affair if problems are encountered and redesign is necessary. Hence, board-level drop tests are first carried out on the PCB with the component attached onto it. The PCB is mounted onto a drop table using screws, and there is no change in its orientation during the test. The impact force causes differential flexing between the board and the chip, thus resulting in failure of the joint (Wong et al. 2002, 2008b).

Solder Materials

Lead-free solder alloys (SAC 305 and Sn–3.5Ag) are identified as lead-free replacements due to their superior creep fatigue resistance. In order to determine the drop impact conditions suitable for these solder alloys, these materials need to be characterized at higher strain rates (Siviour et al. 2005; Wong et al. 2008c). Drop impact strain rates on a joint have been found to range from less than 1–200 s^{-1} (Wong et al. 2008c). Various solder alloys were characterized at strain rates ranging from 0.005 to 300 s^{-1} by Wong et al. (2008c). An Instron micro-force tester was used at strain rates of 0.005 s^{-1} and 12 s^{-1}, while a drop weight tester (involving a drop weight that free-falls onto the test specimen) was developed for strain rates between 50 and 300 s^{-1}(Wong et al. 2008c).

The test results revealed that Sn–3.5Ag and the SAC 305 solders exhibit higher flow stress as compared to that of the Sn–37Pb. Sn–3.5Ag and the SAC 305 solder are also more strain rate sensitive. When solder is reflowed onto a copper pad, it forms a metallurgical joint comprising of the interfacial intermetallic compound (IMC), Cu_6Sn_5. This is a brittle intermetallic compound which fails suddenly when overloaded. The higher flow stress at high strain rates induces stress in the Cu_6Sn_5 IMC as the bulk solder does not yield. For the cases of Sn–37Pb and SAC 101 solders, they exhibit comparable flow stresses which are considerably lower than that of Sn–3.5Ag and the SAC 305 solders. As a result, both Sn–37Pb and SAC 101 solders yield when stressed, resulting in bulk solder failure. The interfacial IMC is not subjected to high stress which causes it to fracture. In the case where drop impact reliability is required, SAC 101 solder is a good replacement to Sn–37Pb solder due to its lower flow stress. Figure 39 shows the stress–strain curves for SAC 101, SAC 305, and eutectic tin–lead solder.

Board-Level Drop Test (BLDT)

The Joint Electronic Device Engineering Council (JEDEC) standard JESD22-B111 (JEDEC Solid State Technology Association 2003) outlines a board-level drop test that is commonly carried out. It specifies the test board thickness and dimensions, layout, and location of components. It recommends using a drop tower with a special base plate for mounting the board with standoffs and four screws – one at each corner. When the base plate is released from a certain predetermined height, it falls freely onto a surface inducing a repeatable impact force on the base plate. For portable mobile products such as mobile phones, the recommended shock pulse on the component is a peak acceleration of 1500G and pulse width of 0.5 ms. A schematic drawing of the setup is shown in Fig. 40.

In the study conducted by Wong et al. (2009), board-level drop tests were carried out on 12 solder material systems consisting of five solder alloys and two pad finishes as shown in Table 12. The cumulative distribution of drops (shocks) to failure for each material system is graphically represented in Fig. 41. Three main conclusions are drawn from this work. Firstly, longer life corresponds to ductile failure, while short life corresponds to intermetallic compound failure. Secondly, as flow stress of the solder increases, the drop test life decreases. Thirdly, doping SAC 101 with minute amounts of Ni is found to enhance the drop test life.

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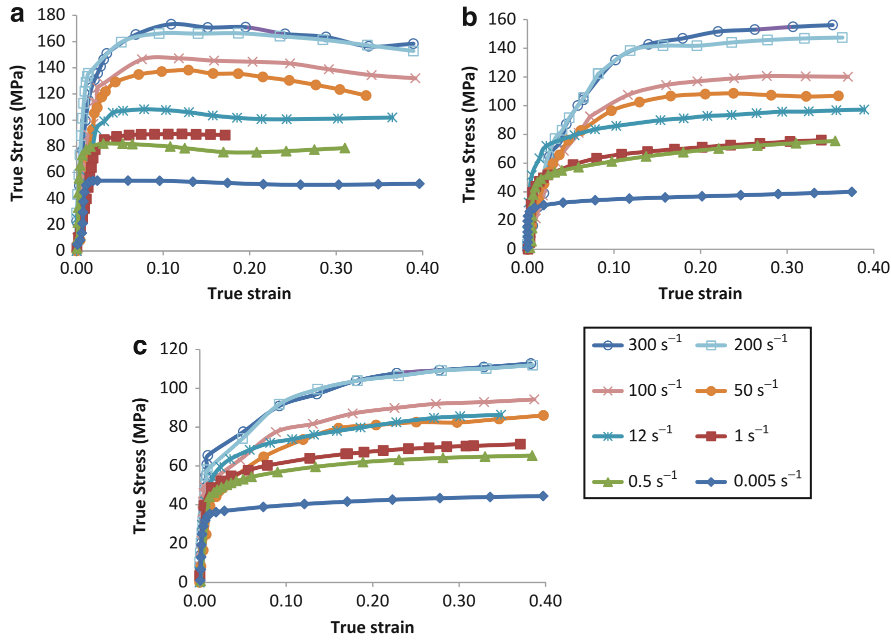

Fig. 39 True stress–strain curves of (**a**) SAC 305, (**b**) SAC 101, (**c**) Sn–37Pb

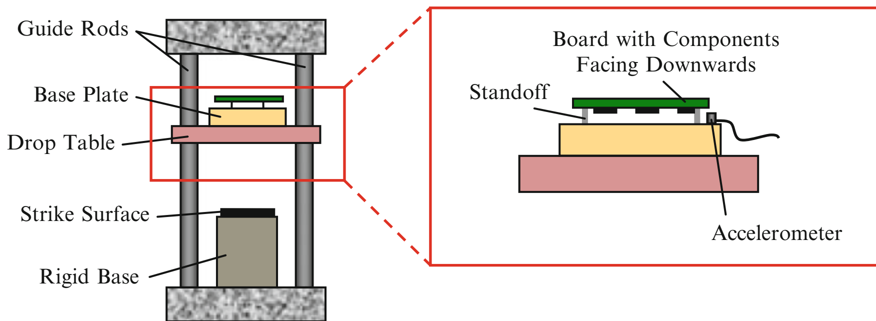

Fig. 40 Schematic drawing of a drop test setup

Table 12 Twelve material systems consisting of six solder alloys and two pad finishes (Wong et al. 2009)

Solder alloy	Pad finish
1. Sn–37Pb (Sn–Pb)	1. Electroless nickel immersion gold (ENIG)
2. Sn–3.5Ag (Sn–Ag)	2. Organic surface preservative over copper (OSP)
3. Sn–1.0Ag–0.1Cu (SAC 101)	
4. Sn–3.0Ag–0.5Cu (SAC 305)	
5. Sn–1.0Ag–0.1Cu with 0.02 % Ni and 0.05 % In (SAC 101(d))	
6. Sn–3.0Ag–0.5Cu with 0.05 % Ni (SAC 305(d))	

High-Speed Cyclic Bend Test (HSCBT)

A tester which applies a sinusoidal cyclic bending directly onto the PCB has been developed by Seah et al. (2006). This tester can apply various bending cycles, each at different amplitudes – just like the load spectrum experienced by the PCB during a drop impact. A schematic drawing of the tester is shown in Fig. 42.

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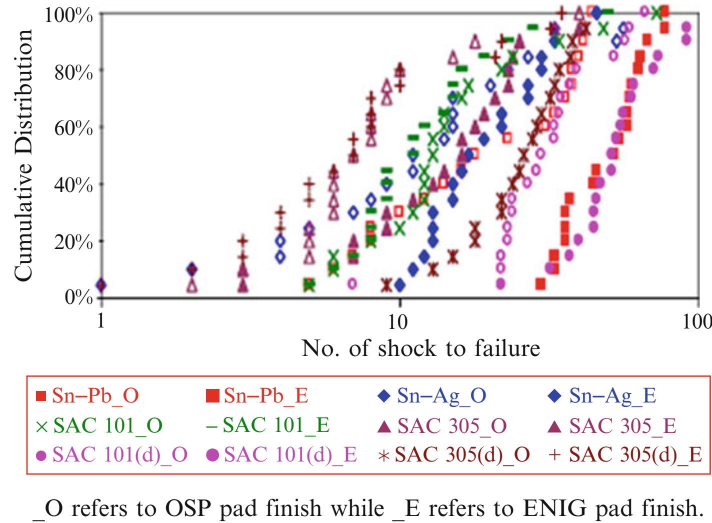

Fig. 41 Cumulative distribution of drop test life for the material systems tested (Extracted from (Wong et al. 2009))

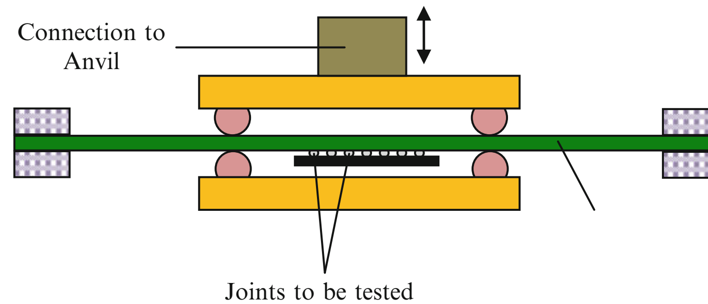

Fig. 42 Schematic drawing of the bend test setup developed by Seah et al. (2006)

The 12 solder systems in Table 12 were subjected to high-speed cyclic bend test (Wong et al. 2009). The resultant cumulative distribution of cycles to failure for the material systems tested is presented in Fig. 43. Results show that this test reproduces the failure modes observed in board-level drop test. There is also a good correlation with the drop test for the 12 material systems studied, in terms of the replication of failure mode and the performance of material systems. The high-speed cyclic bend test is a faster test than the conventional board-level drop test taking into consideration the mode of operation of these two testers.

Ball Impact Shear Test

Conventional solder joint shear tests performed at low speeds induce failure in bulk solder. Ball impact shear test (refer to Fig. 44) uses a high-speed shear tester with solder ball shear speeds of up to 1 ms^{-1}. This high shear speed test induces failure in the brittle interfacial IMC layer of the joint, making this test more suitable than the conventional shear test, where drop impact reliability is a concern.

In this study by Wong et al. (2008a), the 12 material system as listed in Table 12 were subjected to ball impact shear test. The cumulative distributions of the peak load and the total fracture energy is shown in Fig. 45.

Results show that there is no universal correlation between the ball impact shear test and the board-level drop test. This is evidently shown in the material performance results presented in

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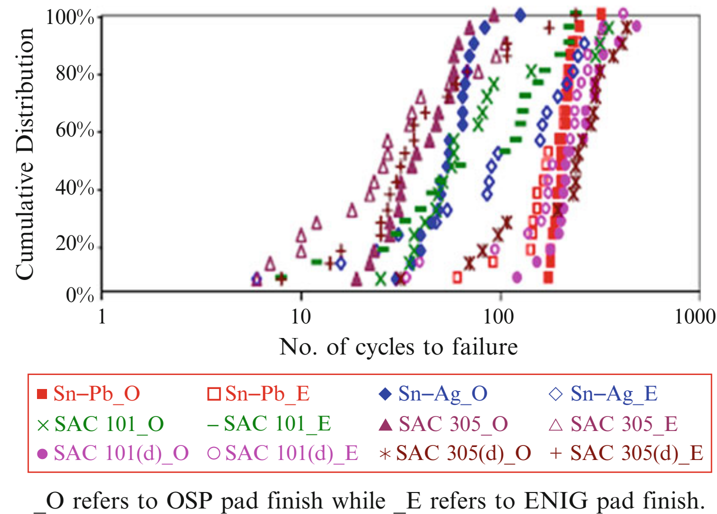

Fig. 43 Cumulative distribution of cycles to failure for the material systems tested (Extracted from (Wong et al. 2009))

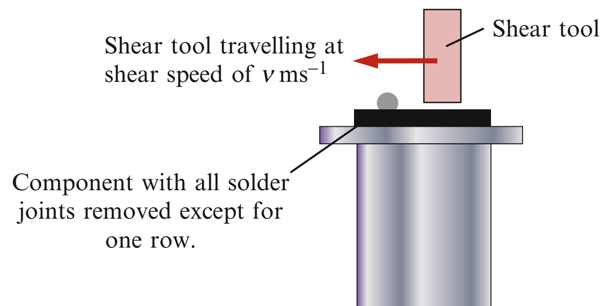

Fig. 44 Schematic drawing of a shear test setup

Figs. 41 and 45. This is because the failure mode in drop test is not consistently reproduced in the shear test. The high-speed shear test is a useful tool for testing quality of solder joints and pad finish in a manufacturing environment.

Mechanical Simulation

Drop impact simulation is also carried out for the purpose of drop life prediction of BGA solder joints (Syed et al. 2007). The steps taken for drop impact simulation are similar to that in temperature cycling. Some aspects of the model such as loading conditions and material properties need to be varied to capture the behaviors of the board and solder joint adequately.

Step 1: Creating the FEA Model

Similar to the temperature cycling simulation, a quarter model of the package is created and meshed.

Step 2: Defining Material Properties

Strain rate-dependent material properties (as shown in Fig. 39) are defined for the solder alloys.

Step 3: Defining Loading Conditions

There have been three methods proposed to define the loading conditions in drop impact, namely, (i) the free-fall of a drop table, (ii) the input-G method, and (iii) the excitation of sample supports. The most tedious is the free-fall of the drop table as it requires the entire test setup to be

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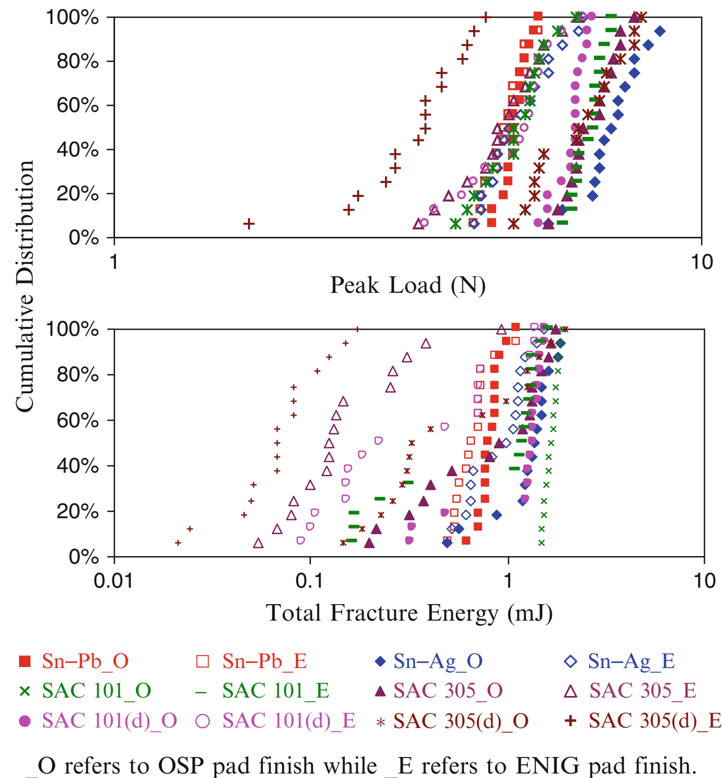

Fig. 45 Cumulative distributions of peak load and total fracture energy for each material system tested (Extracted from (Wong et al. 2008a))

simulated. In this simulation, the drop table with the test board mounted on it using the standoffs is modeled and subjected to a gravity loading. This method is used when the input acceleration pulse is not known.

Tee et al. (Luan and Tee 2004; Tee et al. 2004, 2005) proposed the input-G method. With this method, none of the other supporting structures such as the standoffs or the drop table need to be modeled, thus reducing the computational time greatly. A measured acceleration pulse, or G-level, is applied to the mounting holes of the board.

The other simulation method, developed by Yeh et al. (Yeh and Lai 2006; Yeh et al. 2006), is called the support excitation scheme. Only the test board needs to be modeled. However, instead of applying an acceleration pulse as in the input-G method, body forces are applied to the test board. The body force is the mass matrix of the board multiplied by the acceleration pulse.

Step 4: Analyzing the Results

A suitable parameter such as volume-averaged plastic strain or plastic work at the neck of the solder joint is then correlated to the number of drops to failure.

Step 5: Correlation with Experimental Results

The plastic strain-based life prediction model based on the power law is typically used for cases where failure occurs through bulk solder. This is shown in Eq. 14 (Syed et al. 2007):

$$D_f = A\left(\varepsilon_p\right)^b \tag{14}$$

where D_f is the number of drops to failure, A is a constant, b is an exponent, and ε_p is the plastic

strain. In cases where failure occurs through the intermetallic compound (IMC), the plastic strain in Eq. 14 is replaced by peeling stress (Luan and Tee 2004).

Step 6: Life Prediction

Similar to temperature cycling reliability simulation study, once the constants A and b in Eq. 14 are determined, life prediction can be carried out. FEA models need to be created for the packages in question, and the plastic strain (ε_p) is extracted from the models. Using Eq. 14 and the constants determined in Step 5, the number of drops to failure may be calculated.

Summary

This chapter provides an overview of the role of soldering in electronic packaging and the key soldering processes. Driven by environmental concerns of the use of lead and legislative implementation to ban lead, solder materials evolve from lead-containing to lead-free materials. Furthermore, high-temperature solders and composite solders are developed in recent years to cater to the harsher service and functional requirements of interconnects. The key characteristics which are critical to the reliability and manufacturability of solder materials are also discussed. Lastly, in order to provide a better understanding of the reliability of bulk solder materials and solder joints, reliability studies in terms of mechanical behavior, temperature cycling, and drop impact are discussed in this chapter.

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