RF Interface Design Using Mixed Mode Methodology

Augusto Gallegos[(1)], Philippe Silvestre[(1)], Michel Robert[(2)] and Daniel Auvergne[(2)]
[(1)]VLSI Technology, a subsidiary of Philips Semiconductors CPG - 505, Route des lucioles, 06560 Sophia Antipolis France [(2)]LIRMM, UMR CNRS – Université de Montpellier II – 161, rue Ada, 34392 Monpellier Cedex 5, France

Key words: mixed-signal modeling, RF circuit, DECT system

Abstract: A VHDL-SPICE mixed-signal modeling methodology is applied to the RF interface of a DECT ASIC designed in CMOS 0.35 µm technology. An overview of actual mixed design flows is presented followed by the DECT system description. Then a mixed-signal methodology is introduced to validate the whole circuit behavior. We illustrate the approach with detailed models, simulation results and experimental data. The chip was successfully tested and produced by VLSI Technology.

1. INTRODUCTION

Telecommunication system integration level in ASIC design needs a consistent verification mechanism for complete analog-digital circuits. Thus, efforts to improve IC modeling and verification are essential. The trend of increasing circuit functionalities gives rise to more complex digital-analog interfaces, higher operation frequencies and sophisticated circuit behaviors. Unifying system knowledge with CAD methodologies results in correct realization of these critical designs.

Mixed-Mode design state-of-the-art: Prototyping is a common but expensive verification method used nowadays for complex mixed-signal ASICs. Nevertheless, various CAD tools present faster and less expensive design methodologies:

i. Full-digital design process (*Figure 1*). With CAD advanced development in digital technology, designers choose generally to simulate the full circuit with a digital HDL simulator [1]. Design flows start by the system specification. During this phase, the preliminary analog and digital architectures are defined. The next step is system

The original version of this chapter was revised: The copyright line was incorrect. This has been corrected. The Erratum to this chapter is available at DOI: 10.1007/978-0-387-35498-9_57

L. M. Silveira et al. (eds.), *VLSI: Systems on a Chip*

simulation. Digital parts are then modeled using a standard HDL. Instead, in order to model the analog parts with a digital HDL, the user must define a time domain function, which is a very time consuming task [2]. Besides, the resulting analog model cannot be directly compared to the transistor level description of the circuit using only a logic simulator. Two simulation phases are generally necessary: The behavioral validation and the structural verification. During the first phase, digital models are represented by RTL descriptions and analog parts are modeled with HDL behavioral models. The next steps are digital synthesis, analog layout design, place and route. When the full ASIC layout is available, a back-annotated description for each digital part can be extracted. However, analog circuits have no post-layout model. Consequently, for the structural simulation phase only the behavioral analog descriptions can be used. When this last phase is done, the ASIC is ready to be produced.

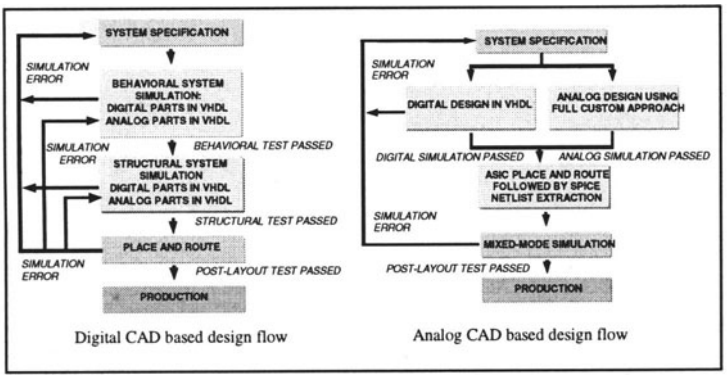

Figure 1. Mixed Mode Design state-of-the-art

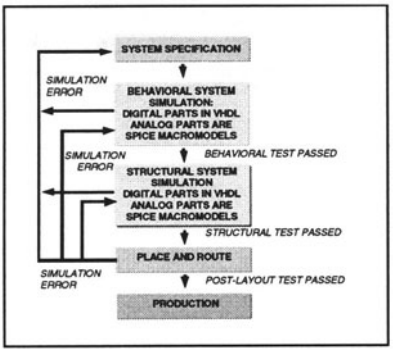

Figure 2. ELDO-QuickHDL Design Flow

ii. Event-driven transistor-level simulation (*Figure 1*). A uniform description of the IC can be obtained at transistor level. Designers verify the SPICE netlist with a simulator based on an advanced electrical simulation approach: The event-driven transistor-level simulation (EDTLS) [3]. The transistor model simulation speed is improved with look-up table methods, spare matrix processing and simplified transistor models. The design flow starts by system specification too. Then the digital and analog elements are separately implemented and simulated. The first integration process takes place during

layout. The mixed signal system simulation is carried out only at the post-layout phase, when all transistor level descriptions are available. System debug needs complete design cycle iterations. Consequently, the methodology is not suitable for short time-to-market ASICs.

In the last few years, CAD tools were introduced to support both, SPICE and digital HDLs [4]. One approach uses a backplane to couple an analog and a digital simulator [5]. This paper presents a design flow (*Figure 2*) and modeling methodology using Mentor Graphics® ELDO-QuickHDL environment. To model digital parts, VHDL behavioral and structural descriptions are built. To represent analog parts, SPICE macromodels are extracted from the transistor level description. Both kinds of models allow accurate and fast system evaluation; thus, the whole architecture is precisely defined after the first simulation phase. The remaining possible defaults are those related to clock-skew for digital circuits and to parasitic resistance and capacitance for analog parts. Only when the system has been fully evaluated, the structural description implementation may start. After final ASIC place and route, the digital part is back annotated. The SPICE macromodels for this phase are extracted from post-layout transistor level netlists. In this way, the final structural simulation targets only timing problems. Usually, this kind of problems doesn't need significant architecture modifications to be solved. As a result, it's not necessary to repeat the full design cycle.

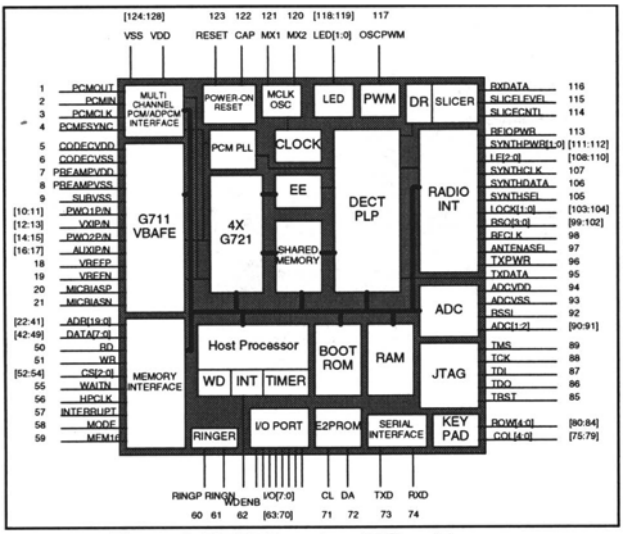

Figure 3. DECT base band IC architecture

2. THE DECT SYSTEM

The DECT (Digital Enhanced Cordless Telecommunications) system allows a 12 full-duplex channel digital wireless communication. TDMA frames are used to set 24 communication slots. Digital data is sent and received at a base band frequency of 1.152 kbps. In Europe, 10 radio carriers are allocated to modulate digital information in the 1800-1900 MHz band. Typical DECT system implementations require a base band processing ASIC and a RF module. *Figure 3* describes the developed base band ASIC architecture, which has been

implemented by VLSI Technology using 0.35 μm CMOS technology. The base band circuit operation (*Figure 4*) is summarized as follows: Audio signal is filtered and converted to PCM data by a Voice Band Analog Front-End circuit (VBAFE). A microprocessor may process this data e.g. for echo cancellation. The G721-coder circuit compresses PCM to ADPCM and stores information in a shared memory. The DECT Physical Layer Processor (DECTPLP) and Encryption Engine (EE) build the TDMA encrypted frame and forward it to an external RF module via a radio interface. The latter is used to illustrate the mixed-signal approach of this paper.

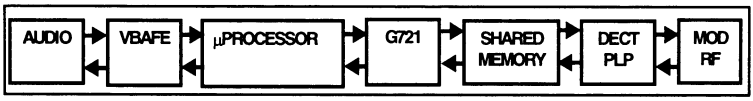

Figure 4. DECT base band processing

3. DECT RADIO INTERFACE

Our approach has been used for the whole chip design. However, this contribution illustrates only how we apply the mixed-mode methodology to the most challenging part, the RF interface. The RF interface architecture (*Figure 5*) is based on a sequencer, the Radio Signal Controller (RSC). A sequence RAM contains the control signal values and the DECT time to set them. DECTPLP provides the current frame timing signals: Slot start, slot stop, DECT bit number, A-Field start, B-Field start, etc. The sequencer sets the control signals following the RAM values, which correspond, to the frame timing. These signals are sent to several digital blocks: the clock recovery circuit, synthesizer programmer and RSSI controller. The analog circuits are the pseudo-gaussian filter, the data slicer and the RSSI ADC, which are also controlled by the RSC. *Figure 5* shaded areas show the analog blocks.

A typical RF IC block diagram is represented in *Figure 6*. GMSK modulation is usually achieved sending the baseband digital data to a gaussian LPF which output drives directly the IF VCO. This signal is then upconverted by a mixer. The Gaussian LPF may also be implemented in the baseband ASIC with look-up tables or any other digital processing method. During demodulation, the RF signal passes through a low-noise amplifier to the IF mixer. The IF signal is then demodulated by a PLL. The demodulated signal must be sliced to recover digital data. Furthermore, data slicing is crucial to clock recovery. The Data Slicer is usually integrated in the base band ASIC. So, mixed-mode modeling must be suitable to correctly analyze the full reception path. Indeed, during reception, several factors need to be considered in addition to the input/output impedance models. The demodulated RF signal contains high-frequency noise and it's affected by multi-path interference. In addition, this data slicer has to be turned on only during the receive slot to save power. The mixed-signal designer may need to test several data slicer architectures. Furthermore, he would rather prefer to use a circuit description close to the real implementation and not just a behavioral model, which performances need to be accurately measured with the original transistor level circuit.

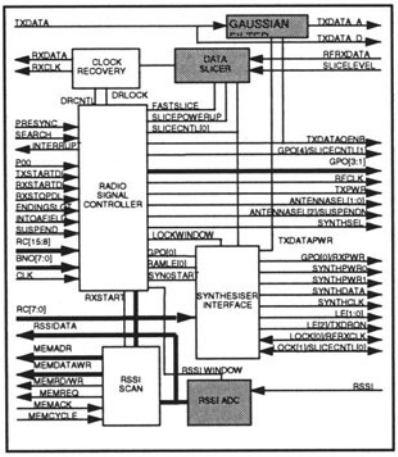

Figure 5. RF interface architecture

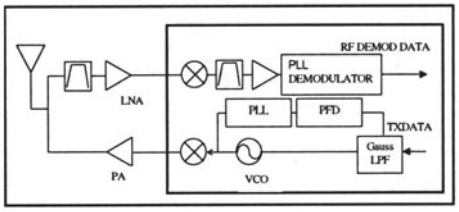

Figure 6. RF IC block diagram

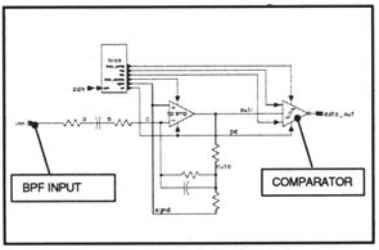

Figure 7. Data Slicer Architecture

4. MODELING APPROACH

The radio interface digital parts at RTL and structural levels are described in VHDL. The analog modeling methodology will be illustrated with the Data Slicer circuit (DS). *Figure 7* shows the preliminary DS architecture, which transistor level description will not be put in layout until the system verification has been correctly achieved. The demodulated RF signal model will be implemented in VHDL using the following equation:

$$g(t) = \frac{K}{2}[erf\{\sqrt{\frac{2}{\ln 2}}\pi B(t-\frac{T}{2})\} + erf\{\sqrt{\frac{2}{\ln 2}}\pi B(t+\frac{T}{2})\}]$$

Where B is the gaussian filter 3-dB bandwidth, T is the DECT pulse width and *erf(x)* is the gaussian error function. The g(t) function is sent to the input of a band pass filter (BPF), which midband is located at 1 MHz is used to remove RF noise. The BPF output is forwarded to a 2-threshold (Thn, Thp) comparator to extract DECT data. This data is forwarded to the clock recovery circuit and both, data and clock signals are provided to DECTPLP circuit that processes the TDMA frame. The BPF transfer function is:

$$F(s) = \frac{a_2 s^2 + a_1 s^2 + a_0}{b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s^2 + b_0}$$

Where: $a_0 = -0.31022 \times 10^{10}$, $a_1 = -0.13665 \times 10^{14}$, $a_2 = -0.49055 \times 10^{5}$, $b_0 = 0.62986 \times 10^{19}$, $b_1 = 0.30249 \times 10^{13}$, $b_2 = 0.297201 \times 10^{6}$, $b_3 = 0.927115 \times 10^{-2}$, $b_4 = 0.354149 \times 10^{-10}$, $b_5 = 0.1 \times 10^{-18}$. Such function would represent a difficult modeling task using a digital HDL. The

macromodel in ELDO, for the whole data slicer (BPF and the comparator) is implemented as shown in

Table 1.

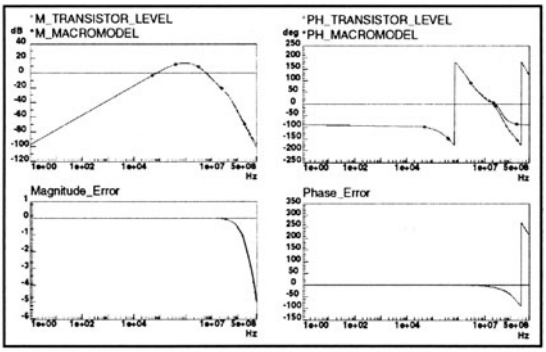

Figure 8. AC analysis

ELDO Pole-Zero Post-Processor extracts the FNSfilter model from the BPF architecture. This model represents the correct behavior within the DECT bandwidth as shown by the error curves (*Figure 8*). An ELDO macromodel (ytrig) is used to model the 2-threshold comparator architecture. Note that the slicer output and input, *a_out* and *inn* respectively, are mixed-signal nodes that exchange data between ELDO and the digital simulator QuickHDL. We assume that the RF demodulator output has a very low impedance compared to *inn*, so we didn't implement a more complex A-to-A interface description, like a voltage controlled source. If this were required, it would be a very simple task using the SPICE language. The whole model was implemented and evaluated in few hours. In addition, it's not a transistor level description neither a complex mathematical formula, which are difficult to analyze and debug. The simulation speed has been 50-fold improved.

Figure 9 shows the mixed-mode system testbench, where only the main blocks have been represented. For the first mixed-signal simulation phase, all digital parts (DECTPLP, CR, Shared RAM, RISC processor etc.) are available in VHDL RTL descriptions. The analog SPICE macromodels are those extracted before the analog layout implementation. The microprocessor initializes the system and the DECT reception starts running as shown in *Figure 4*. As the test module sends the RF signal of demodulated data, the DS and clock recovery (CR) circuits restore digital data for the DECTPLP. The latter detects the synchronization field for each slot to freeze CR clock phase and also recovers B-Field data storing it in the shared memory. *Figure 10* displays the simulation results computed with the preliminary DS architecture. The test module data sent in digital and analog forms, **TESTBENCHDATA** and **SLICE_IN** respectively, is compared to the recovered data **SLICE_OUT**. For the preliminary DS architecture, the synchronization field (E89Ah) after the preamble pattern (AAAAh) is not correctly recovered. After the system

behavior analysis, the DS has been completely redefined. At this design phase the DS circuit can be modified and validated without involving layout design. The final DS circuit includes a DC offset latch circuit. *Figure 11* shows the correctly recovered **SP_MACR_RXDATA** signal, where **V(SLICEIN)** is the RF demodulated data and **SP_MACR_VC** is the latched offset value. Results are directly compared to experimental data. A mixed-mode test done for one DECT frame needs 20 min. The same simulation bypassing analog circuits, thus using only QuickHDL logic simulator, takes 5 min. This proves that simulation speed is affordable for complex system evaluations.

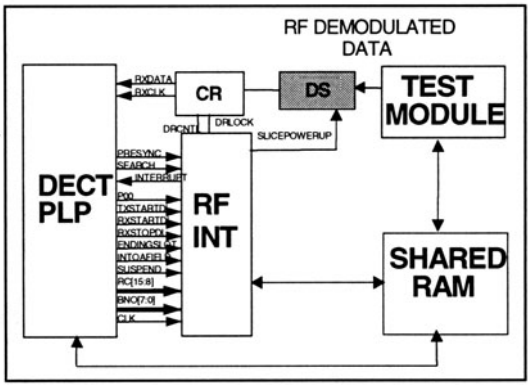

Figure 9. Mixed-Signal Testbench

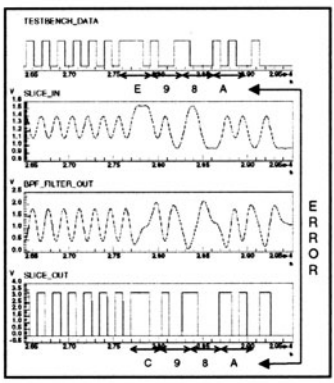

Figure 10. Simulation result: Error detection

Table 1. Data Slicer macromodel

```
FNS_MACROSPICE data slicer
Vrefere      refv        0     3.3
Voffs        outioff     0     1.1314E+00
Roffs        outioff     0     1
FNSfilter  inn outiac
+ -0.310225E+10 -0.136656E+14
+ -0.490556E+05
+ ,
+  0.629860E+19  0.302495E+13
+  0.297201E+06  0.927115E-02
+  0.354149E-10
+  0.100000E-18
yoffs add pin: outiac outioff outi
ytrig lev_d outi 0 outp outn refv
+ param: tr=9.54E-11 tf=6.5E-11
+ tpd=33.3E-09 v0=0 v1=3.3 voff=0
+ vrl=1.2309E+00 vru=1.0302E+00
.connect outn a_out
.model model_rd2a dtoa MODE=REAL
.D2A SIM=BP inn     MOD=model_rd2a
.model model_a2d atod MODE=MVL9
+ VTH1=1.0 VTH2=2.0
.A2D SIM=BP a_out MOD=model_a2d
.end
```

5. CONCLUSIONS.

The presented hierarchical modeling approach was used to design a DECT ASIC in CMOS 0.35 μm technology, ensuring circuit quality with full system simulations and improving dramatically the time-to-market, due to an early validation procedure. We compared simulation results to experimental data to prove the methodology validity as the presented circuit has been successfully tested and produced by VLSI Technology Inc. (part no. VP40553). Future works may extend models to include multi-path interference effects, noise and other RF module characteristics.

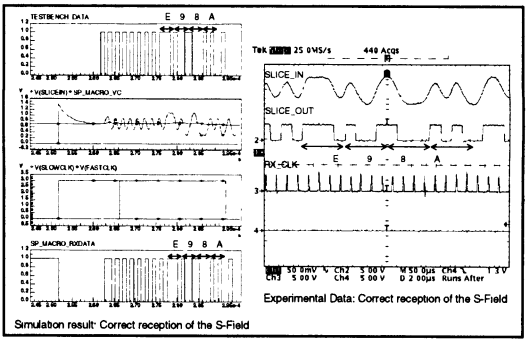

Figure 11. Mixed-Mode simulation results comparison to experimental data

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