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From Lattices to Practical Formal Hardware Verification

(Invited Lecture)

C. Seger
Strategic CAD Labs, Intel Corporation
5200 N.E. Elam Young Pkwy.
Hillsboro, OR 97124-6497 USA
cseger@ichips.intel.com

Abstract

Symbolic Trajectory Evaluation (STE) is a model checking algorithm that mixes the use of lattice structures with binary decision diagrams. In addition to this algorithmic decision procedure for the logic, there is also a sound and complete set of inference rules for the logic. Together, these make STE an attractive candidate for a verification system. In this talk we will briefly introduce the underlying theory of STE. We will then discuss the challenges we faced in making STE the basic model checker in the Voss hardware verification system and how the inference rules were used to extend the capabilities of the system. The emphasis of the talk will be on the process of taking a nice theory and making it practically useful.

BIOGRAPHY

Dr. Carl Seger received his M.A.Sc. in Engineering Physics from Chalmer's University of Technology, Sweden, in 1985 and his M.Math and Ph.D. degrees in Computer Science from the University of Waterloo, Canada, in 1986 and 1988 respectively. After two years as Research Associate at Carnegie Mellon University he became an Assistant Professor in the Department of Computer Science at the University of British Columbia, Canada, and in 1995 he became Associate Professor. He was a visiting professor at Intel in the summer of 1995 and joined Intel full time in December 1995. Dr. Seger's main research interests are formal hardware verification and asynchronous circuits. He is the author of the Voss hardware verification system and is co-author of *Asynchronous Circuits* (Springer Verlag, 1995).

Programming Concepts and Methods D. Gries, & W-P. de Roever (Eds.)