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Low-voltage current-mode analogue continuous-time filters

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Abstract

A novel current-mode analogue continuous-time filter synthesis technique is proposed based on a transformed set of state-equations, that allow the utilization of only current-mode linear lossy-integrators implemented using standard current mirrors; also a novel current-mode gyrator is introduced. The technique has been successfully used for synthesizing low-voltage 5th order lowpass, highpass, bandpass and stopband Chebyshev filters from passive doubly loaded ladder prototypes. SPICE simulations using CMOS standard process level 2 parameters have shown these filters perform well, exhibiting a THD less than 1% at 100 kHz for a 40 mV output (1 μA input current) while the bias current per transistor is 10 μA. Also, a Monte Carlo analysis has shown these filters preserve the low sensitivity inherent to the passive ladder prototype. The reduced number of small transistors necessary leads to small integration areas. The circuits have been fed with ±1.5 V power supplies.

INTRODUCTION

Analogue continuous-time filters can be synthesized from passive doubly loaded ladder networks, preserving their low sensitivity to component variations. For integrated circuit implementations, inductors and resistors can be replaced by using active simulation techniques based on voltage-controlled current-sources (VCCS); operational transconductance amplifiers (OTA) have been successfully used as linear VCCS, originating the so-called OTA-C filters (Queiroz, 1988; Queiroz, 1989), widely used in high-frequency applications.

Analogue continuous-time current-mode filters are commonly synthesized from passive models applying the same techniques and the same state-equations used in synthesis of OTA-C filters. In this way, it is always necessary to use current-mode lossless-integrators made by feeding current into a linear capacitor and then

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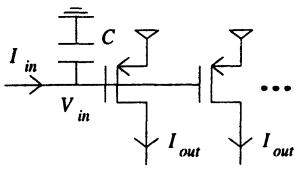
converting the voltage across the integrating capacitor to current, usually through a non-linear operator performed by a single MOSFET (Smith, 1996; Masry, 1996).
In this paper, a novel current-mode filter synthesis procedure is proposed based on a transformed set of state-equations that allow the utilization of only current-mode linear lossy-integrators, based on current-controlled current-sources (CCCS); neither current to voltage nor voltage to current non-linear conversions are necessary (Gálvez-Durand, 1996).
The resulting filter topologies allow the utilization of low-voltage power supplies and can be interesting for those applications where the power consumption must be kept low. Lowpass, highpass, bandpass and stopband filters can be synthesized using this technique, exhibiting a very good performance despite the reduced number of small transistors necessary for these implementations.

MOSFET-C INTEGRATORS

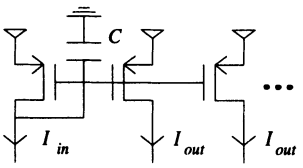
The MOS transistor can be used as building block for current-mode VCCS-based lossless-integrators as well as for CCCS-based lossy-integrators. The first one can be commonly found in analogue current-mode continuous-time filter implementations as a consequence of the synthesis methods applied so far.
For the sake of simplicity, all n-MOS transistors working as bias current-sources are omitted in all figures shown in this paper. Also, the non-linear second order effect introduced by the MOSFET output channel-conductance is neglected in all the algebraic analysis (but it will be taken into account in all simulations present hereafter).
A current-mode VCCS-based lossless-integrator is usually implemented by a non-linear function $f(\bullet)$ performed by a single MOSFET. A p-MOS implementation of such a current-mode non-linear lossless-integrator is depicted in figure 1.



$$I_{out} = f\left(\frac{I_{in}}{sC}\right)$$

Figure 1 Current-mode non-linear lossless-integrator

A linear CCCS-based lossy-integrator can be implemented using standard current mirrors, figure 2. The cutoff frequency of this integrator is given by *gm/C*, where *gm* is the input MOSFET transconductance and C is the integrating capacitor.



$$I_{out} = -\frac{I_{in}}{s\frac{C}{gm}+1}$$

Figure 2 Current-mode linear lossy-integrator

For these two integrators, the most important MOSFET parasitic component is the gate-to-source capacitor; the channel drain-to-source conductance is also important but its effect can be minimized by using more complex MOSFET structures (Gálvez-Durand, 1994).
In the sake of simplicity, the MOSFET's transconductance is going to be normalized to one (gm =1) in all the analysis performed here.

SYNTHESIS

The synthesis technique proposed in this paper is based on a doubly loaded ladder network modified set of state-equations; the implementation of these equations can be performed by using the two MOSFET-based building blocks shown in figure 3.

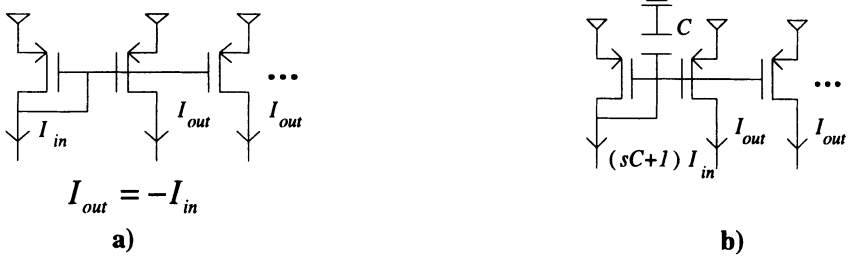


Figure 3 Building blocks: current-mode inverter a) linear lossy-integrator (b

The first one is a current inverter performed by a single current mirror, figure 3.a. The second one is a current-mode lossy-integrator performed by a single current mirror and a linear capacitor C attached to its common-gate node, figure 3.b.
The proposed synthesis technique can be introduced using the lowpass case as example.

Lowpass

The passive ladder network in figure 4, has been obtained from a generic 5th order lowpass approximation without finite zeros.

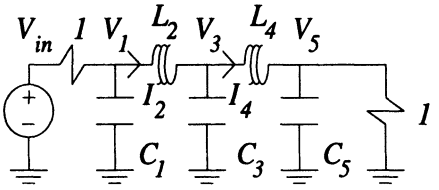


Figure 4 A 5th order lowpass passive doubly loaded ladder network without finite zeros

The state-equations for the prototype in figure 4 are usually written out taking as state variables all capacitor voltages and inductor currents. In OTA-C implementations, all inductor currents are converted to voltages using gyrators; hence, in that implementations all state-variables are voltages and every integration can be performed using linear OTA-C lossless-integrators.

$$
\begin{aligned}
sC_1V_1 &= V_{in} - V_1 - I_2 && (a)\\
sL_2I_2 &= V_1 - V_3 && (b)\\
sC_3V_3 &= I_2 - I_4 && (c)\\
sL_4I_4 &= V_3 - V_5 && (d)\\
sC_5V_5 &= I_4 - V_5 && (e)
\end{aligned}
\qquad (1)
$$

In this way, a lossless integration implies always in performing a voltage to current and then a current to voltage conversion. However, all lossless-integrators in eq. 1 can be converted to lossy-integrators by adding dummy terms to both sides of eq. (1.b), (1.c) and (1.d); integrators in eq. (1.a) and (1.e), corresponding to state-capacitors C_1 and C_5, are already lossy due to the passive network resistive loads. Then, eq. 1 can be rewritten in the lossy-integrators form of eq. 2.

$$
\begin{aligned}
(sC_1 + 1)V_1 &= V_{in} - I_2 && (a)\\
(sL_2 + 1)I_2 &= V_1 - V_3 + I_2 && (b)\\
(sC_3 + 1)V_3 &= I_2 - I_4 + V_3 && (c)\\
(sL_4 + 1)I_4 &= V_3 - V_5 + I_4 && (d)\\
(sC_5 + 1)V_5 &= I_4 && (e)
\end{aligned}
\qquad (2)
$$

Realizing all state-variables as currents instead of voltages, the eq. 2 can be implemented using the building-blocks in figure 3.
The block in figure 5, is a novel structure for a current-mode gyrator, capable of generating the state variables representing the lowpass passive ladder prototype inductor currents. This circuit uses: the current-mode lossy-integrator in figure 3.b loaded with a capacitor of the same value as the L_j inductor's, the current inverter in figure 3.a and the state-variables V_i and V_k (now represented by currents), proportional to the voltages across the inductor L_j in the passive prototype. This block can implement eq. (2.b) and (2.d).

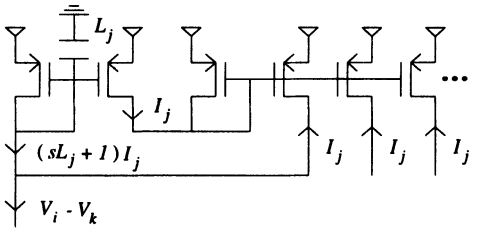


Figure 5 Current-mode gyrator for lowpass filters

The current inverter (figure 3.a) used in the current-mode gyrator in figure 5 introduces a parasitic lossy-integration due to the gate-to-source capacitors of all MOSFET in the current inverter structure. Fortunately, lowpass filter prototypes (of any odd order) synthesized using the technique proposed here do not need current-mode gyrators with more than two output currents. Hence, the effect of this parasitic lossy-integration on the current-mode gyrator performance can be neglected.

Generalized technique

The technique used in the lowpass synthesis can be extended to highpass, bandpass and stopband filters. These filters can be generated by applying frequency transformations to the modified lowpass state-equations (eq. 2).
The eq. 2 can be written out in the generic form shown in eq. 3 where the capacitive susceptances sC_j have been replaced with generic admittances Y_j.

$$
\begin{aligned}
(Y_1 + 1)V_1 &= V_{in} - I_2 && (a)\\
(Y_2 + 1)I_2 &= V_1 - V_3 + I_2 && (b)\\
(Y_3 + 1)V_3 &= I_2 - I_4 + V_3 && (c)\\
(Y_4 + 1)I_4 &= V_3 - V_5 + I_4 && (d)\\
(Y_5 + 1)V_5 &= I_4 && (e)
\end{aligned}
\qquad (3)
$$

The frequency transformations applied to eq. 3 for the synthesis of highpass, bandpass and stopband filters modify the admittances Y_j. The generalization of the synthesis technique introduced in section 3.1 is based on building-blocks capable of implementing the generic terms Y_j +1 for every lossy-integrator necessary in the synthesis of a given filter. In the most simple case, corresponding to the lowpass synthesis, the admittance Y_j simplifies to the susceptance sC_j.
Also, the lowpass current-mode gyrator in figure 5 can be defined as a generic integrator (depending on Y_j +1) and a unit-gain current-mode amplifier, figure 6.

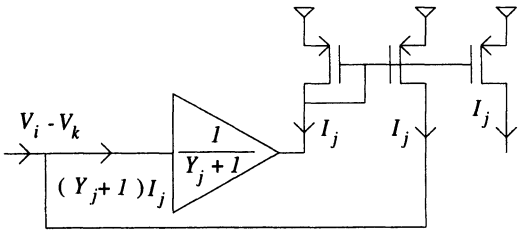
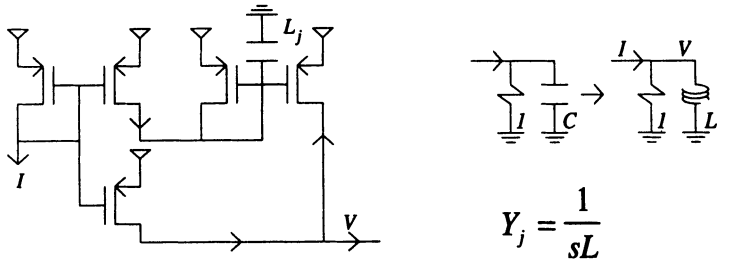
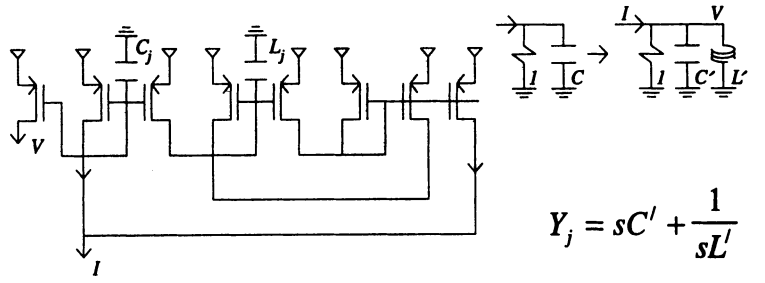


Figure 6 Generic current-mode gyrator

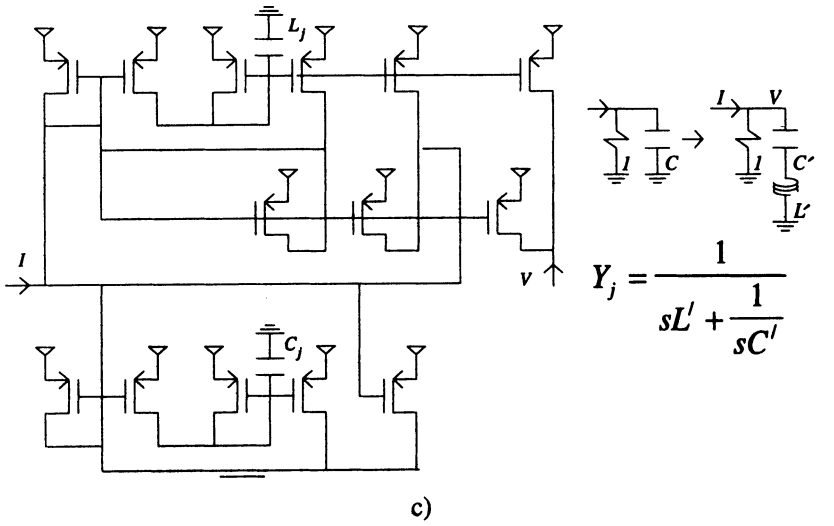
In this way, the synthesis of any filter reduces to designing an adequate integrator. The figure 7 summarize the frequency transformations, the necessary admittances Y_j and the corresponding integrator building-blocks for highpass, bandpass and stopband filters.



a)



b)



c)

Figure 7 Current-mode integrators for highpass a) bandpass b) and stopband c) filters

EXAMPLES

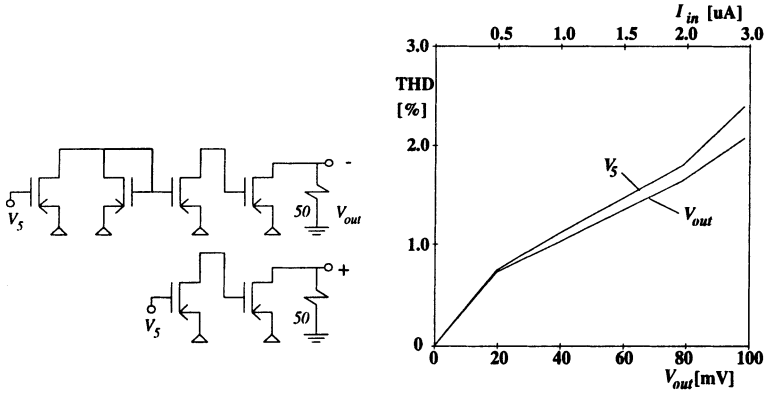
A lowpass and bandpass 5th order 100 kHz, 1 dB passband ripple Chebyshev filters were synthesized using the current-mode technique proposed here.The results were obtained using SPICE level 2 MOSFET model and parameters for a double metal, double poly, n-well, 1.2μm standard CMOS process (threshold voltage n-MOS = +0.68 V, p-MOS = -0.69 V). Both circuits were fed with ±1.5V.

A Monte Carlo analysis was performed varying all transistor dimensions in 100 trials, accordingly to a 2% standard deviation Gaussian distribution. The mean of the filter responses, computed from the 100 Monte Carlo trials in the same figure, exhibits a good performance preserving the passive prototype low sensitivity.

The results obtained scaling these filters to lower frequencies compares advantageously to the results shown here; at lower frequencies transistors with longer channels can be used, reducing the MOSFET output conductance effect.

A differential output buffer, figure 8, is necessary to allow experimental measurements on these prototypes (Gálvez-Durand, 1996). The THD after the output buffer (taken from the 100 Monte Carlo trials mentioned before) is about 1% for a 40mV output signal.

For large output signals the THD at V_{out} is lower than at V_5, because the even order harmonics are canceled. For small output signals the THD for both nodes is almost the same and the relation between the input current and the output voltage can be considered linear ($I_{in} < 2$ μA).



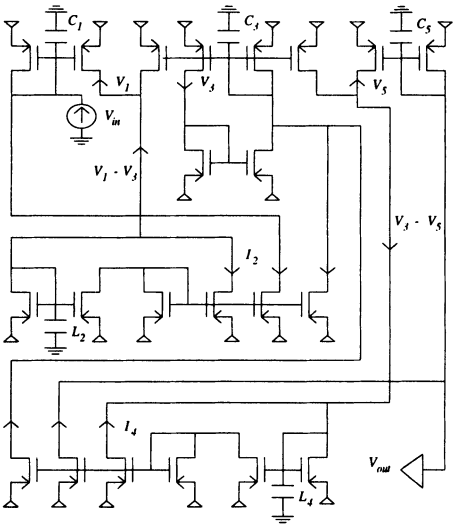
a) b)

Figure 8 Differential output buffer schematic a) The THD before (V_5) and after (V_{out}) the buffer, has been taken from 100 Monte Carlo trials b); the upper horizontal scale shows the input current corresponding to the output voltage in the lower horizontal scale.

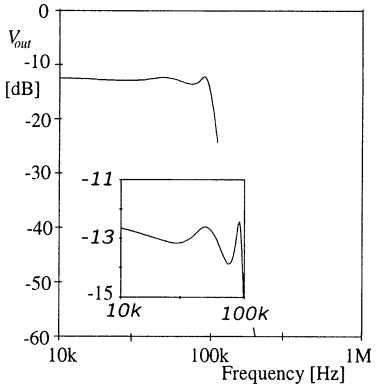
Fortunately, the signal to noise ratio at V_{out} is about 26 for a 40 mV signal, making possible to perform clear measurements in the region where the suppression of even order harmonics introduced by the differential output buffer can be neglected.

Lowpass filter

The lowpass filter power consumption is about 660μW; only 22 pMOS transistors driving signal were used. All pMOS transistors were biased with 10μA currents.



a)



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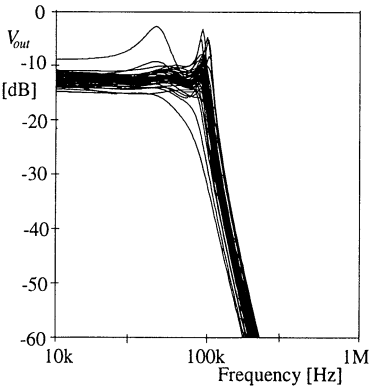


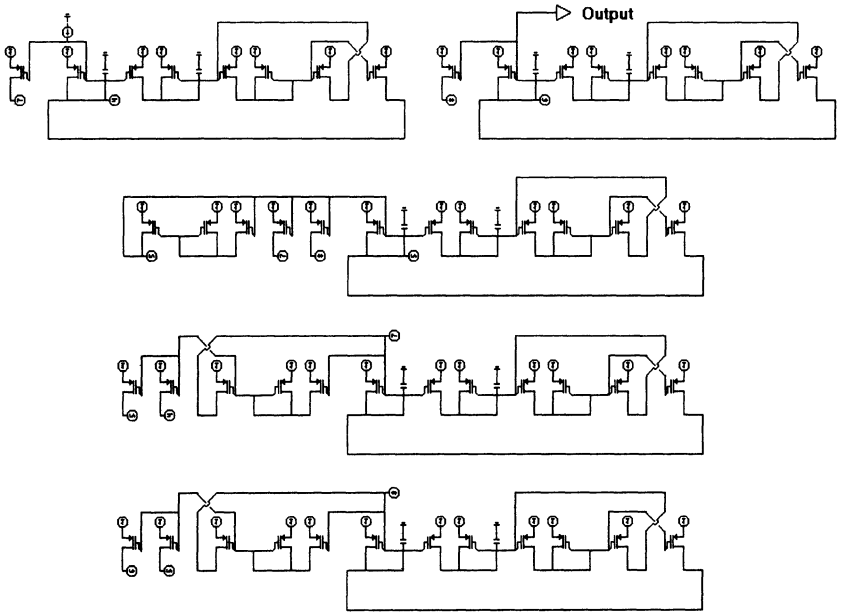
c)

Figure 9 Fifth order 100kHz lowpass Chebyshev filter schematic a). The mean b) for each filter transfer was taken from 100 Monte Carlo trials c).

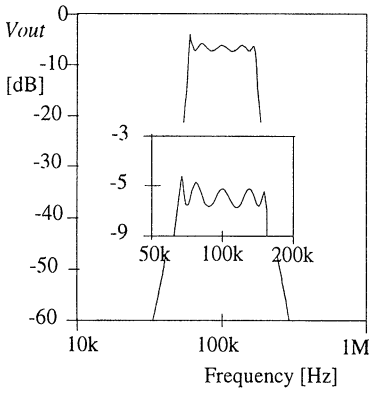
The THD for these filters (assuming perfect matching for all MOSFET) is less than 0.7% for a 40mV output signal (1μA input current), computed at 100kHz without output buffer, that is, about 50% the THD obtained using Monte Carlo analysis for simulating MOSFET mismatches.

Bandpass Filter

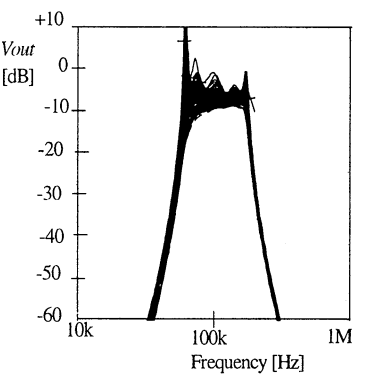
The bandpass filter in figure 10 has a power consumption of 1590μW, using 53 pMOS driving signal. Again, all pMOS transistors were biased with 10μA currents.



a)



b)



c)

Figure 10 Fifth order 100kHz bandpass Chebyshev filter schematic a) the mean b) for the filter transfer was taken from 100 Monte Carlo trials c).

The labels inside the picture have been simplified because of size limitations.
The differential output buffer in figure 8 has been used for this filter too., with similar performance. The filter dynamic range has been equalized only for the 3 states representing the passive prototype inductor currents.

CONCLUSIONS

The current-mode filters generated using the proposed technique are capable of working fed by a 3V low-voltage power supply exhibiting desirable low power-consumption and harmonic distortion (THD).
The signal to noise ratio computed after the differential output buffer allows clear measurements on these prototypes.
A novel generic structure for current-mode gyrators has been presented here; this structure makes possible current-mode simulation of inductors without using neither non-linear current to voltage nor voltage to current conversions.
Also, this structure allows filter implementations of orders higher than 5th without increasing the feedback-between-states complexity.
The results shown here can be applied to even order approximations too, using Moebius transformations for obtaining adequate passive doubly loaded ladder prototypes.
The Monte Carlo analysis has shown the lowpass and bandpass filters reliability even using a standard CMOS integration process. The 2% Gaussian distribution used in this analysis covers errors due to precision in poly and diffusion rectangles and has to do with filter sensitivity (to small flaws), usually computed by SPICE (and other simulators) linearizing the circuit around a bias point and then performing sensitivity analysis using MOSFET's small-signal model. The Monte Carlo method improves these kind of analysis by forcing SPICE to generate a new bias point for every modified circuit (hence, new small-signal components); the raw-data generated is statistically post-processed for obtaining a mean for the desired circuit transfer.
For process and temperature effects (large variations) the filter must be simulated including a master bias-control, responsible by compensating for these effects. A master bias-control shall be designed after obtaining experimental data for these prototypes.
The reduced number of small transistors needed implies in a reduced active fabrication area.
The study of BJT-based building blocks for the implementation of modified state-equations based on lossy-integrators is underway.
The behaviour of these structures with power supplies lower than 3V is also being studied for very low frequency filters.

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