11

A Programmable Second Generation SI Integrator for Low-Voltage Applications

F.A. Farag, R.Faustino, S. Noceti Filho, C. Galup- Montoro and M. C. Schneider

LINSE - Departamento de Engenharia Elétrica - Universidade Federal de Santa Catarina - CEP 88.040-900 - Florianópolis - SC - Brasil - E-mail: carlos@linse.ufsc.br

Abstract

A second generation integrator based on the switching current memory cell reported in (Gonçalves, 1996 A) has been prototyped. The constant voltage switching of the integrator is well suited to low voltage applications, since it avoids the conduction gap of the switches as well as the signal dependent charge injection. A programmable biquad has been implemented using the proposed second generation integrator. The center frequency and the quality factor can be tuned independently.

Keywords

Switched current circuits and Digital programmable filter.

VLSI: Integrated Systems on Silicon R. Reis & L. Claesen (Eds.)

1 INTRODUCTION

Sampled data circuits have been intensively employed in VLSI chips. The switched capacitor (SC) technique has been the prevailing one over the last two decades. SC filters achieve a high accuracy with a low distortion. However, besides requiring a double poly process, the standard SC technique has the problem of increasing prohibitively the resistance of the switches for low voltage operation (Crols, 1994). If the supply voltage is lower than a certain minimum value, the switch resistance tends towards infinity (Crols, 1994 and Vittoz, 1994) for a range of the input level. This "conduction gap" is a critical limitation for SC filters. There are some special techniques to deal with this problem, such as the use of dedicated processes, on-chip generation of a voltage larger than the power supply and the switched op-amp (Crols, 1994). Of course, these techniques add some extra cost to the chip.

In the late 1980s a new sampled data technique called switched current (SI) was introduced (Hughes, 1989 and 1990). The basic SI circuit is the current mode track and hold circuit shown in Figure 1(a). This technique presents the same limitation of SC circuits with respect to the conduction gap of the switches when operated at low supply voltages. To overcome the problem of the conduction gap of the switches, the SI mirror scheme shown in Figure 1(b) was presented in (Gonçalves, 1996 A).

In this work we propose a second generation SI integrator. In the new integrator the switches operate at constant voltage, thus avoiding the conduction gap existing in conventional SI circuits. Moreover, the charge injected by the switches becomes signal-independent. The proposed integrator has been prototyped and programmed by using MOSFET-Only Current Dividers (MOCD) (Bult, 1992 and Gonçalves, 1996 A). A programmable integrator-based biquad which allows independent tuning of the center frequency and the quality factor has been implemented.

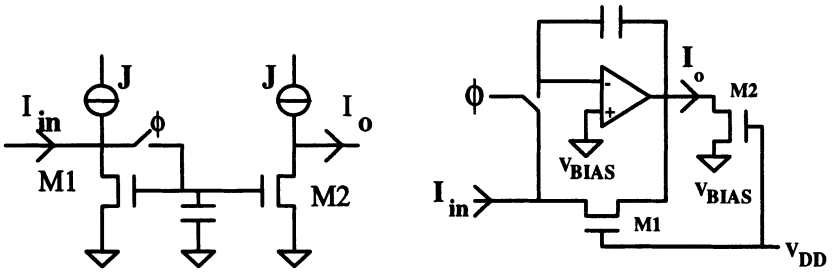


Figure 1 (a)Conventional SI mirror.
(b) SI mirror proposed in (Gonçalves, 1996 A).

2 SECOND GENERATION (SI) INTEGRATOR

The conventional second generation SI integrator (Hughes, 1989) is shown in Figure 2(a). In this paper, we propose a second generation SI integrator based on the SI mirror shown in Figure 1(b). The integrator is made up of two switched current memory cells, as shown in Figure 2(b). Two available outputs are I_{OA} and I_{OB}.

In the odd phase :

$$I_{OA}(n) = \alpha I_A(n) = -\alpha\{I_{in}(n) + I_B(n)\} \qquad (1.a)$$

while in the even phase

$$I_B(n-1/2) = I_B(n-1) = -I_A(n-1) \qquad (1.b)$$

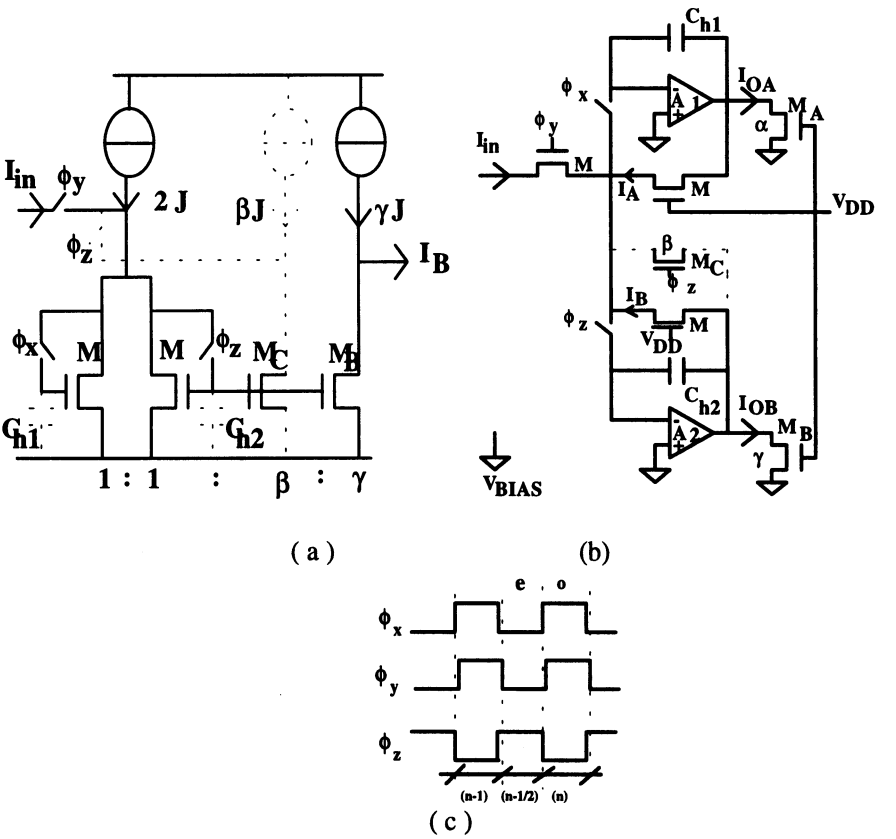


Figure. 2 - (a) Conventional second generation SI integrator.
(b) Proposed second generation SI integrator.
(c)Switching clock sequence.

From equations (1.a) and (1.b) we can write

$$I_{OA}(n) = -\alpha I_{in}(n) + I_{OA}(n-1) \tag{2.a}$$

and

$$I_{OB}(n) = \gamma I_{in}(n-1) + I_{OB}(n-1) \tag{2.b}$$

where $\alpha = (W/L)_{MA}/(W/L)_M$ and $\gamma = (W/L)_{MB}/(W/L)_M$.
W and L are the width and length of the channel, respectively.
The z-transformation of (2.a) and (2.b) gives:

$$\frac{I_{OA}^{\phi_o}}{I_{IN}^{\phi_o}} = -\alpha \frac{1}{1-Z^{-1}} \tag{3.a}$$

$$\frac{I_{OB}^{\phi_o}}{I_{IN}^{\phi_o}} = \gamma \frac{z^{-1}}{1-Z^{-1}} \tag{3.b}$$

The timing of the clock waveforms is shown in Figure 2 (c). This switching sequence is necessary to avoid the loss of information during clock transition in a practical implementation.
A lossy SI integrator can be realized using the dotted feedback path shown in Figure 2 (b). The z-domain transfer functions are:

$$\frac{I_{OA}^{\phi_o}}{I_{IN}^{\phi_o}} = -\alpha \frac{1}{1+\beta-Z^{-1}} \tag{4.a}$$

$$\frac{I_{OB}^{\phi_o}}{I_{IN}^{\phi_o}} = \gamma \frac{z^{-1}}{1+\beta-Z^{-1}} \tag{4.b}$$

where $\beta = (W/L)_{MC} / (W/L)_M$.

The proposed second generation SI integrator has the same sensitivities to transistor mismatches as the conventional SI integrator (Hughes, 1989).

3 EXPERIMENTAL RESULTS

The SI lossy integrator shown in Figure 2 (b) was implemented using operational amplifiers TL 082, MOS integrated transistors (W=48μm, L=1.2 μm), MOS switches CD 4007 and holding capacitors of 1.8nF. The loss factor (β) was set by a 6-bit MOSFET-Only Current Divider (MOCD) (Bult, 1992) whose scheme is shown in Figure3 (a). The 6-bit MOCD was integrated on a Sea of Transistors

(SoT) array, in a 1.2μm technology from ES2 (Gonçalves, 1996 B). The MOCD layout is shown in Figure 3 (b).

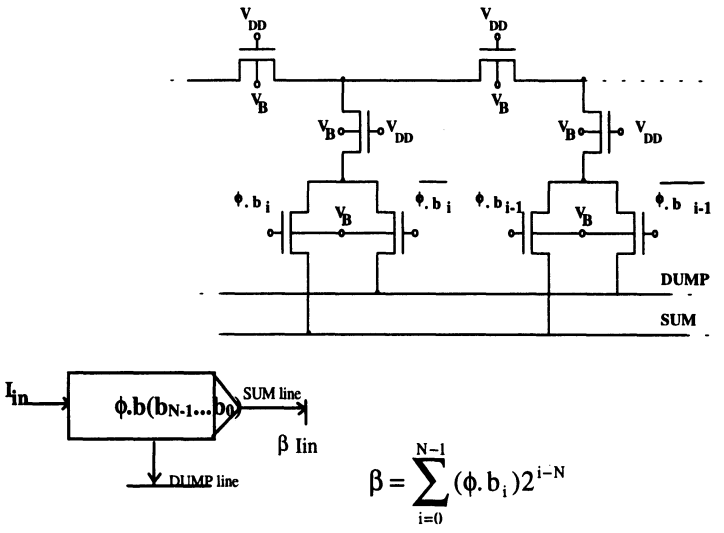
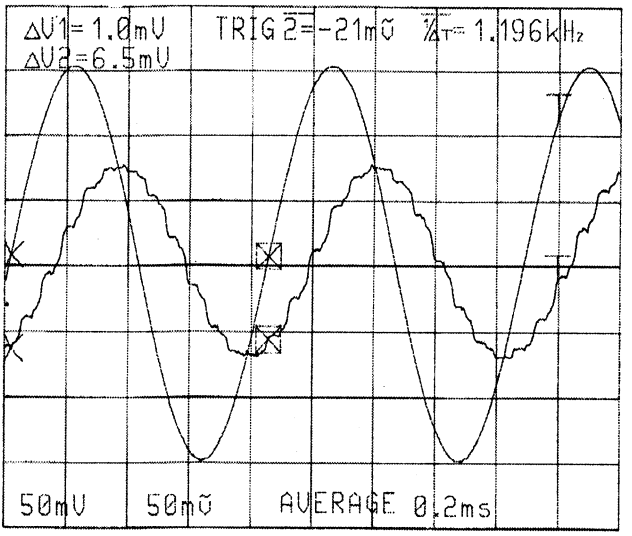
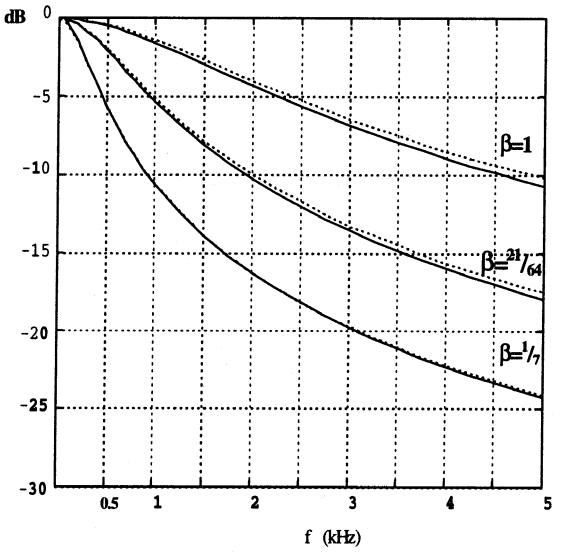


Figure 3 (a)Switched MOCD and Its Symbol.
(b) MOCD layout on an SoT array.

The MOCD input impedance is independent of both the digital word and the clock phase, thus providing a constant load impedance to the op amps. The MOCD is switched by "ANDing" the digital word and the even phase waveforms $\{\phi_e.\mathbf{b}(b_{N-1} \ldots\ldots b_o)\}$. The experimental time response of the integrator is shown in Figure 4 (a) (β=21/64) for a 1.196kHz input signal. Note that the output signal does not present glitches. This important property is due to the constant voltage switching of the memory cell. The integrator has been simulated using the ASIZ program (Queiroz, 1993). The simulated and experimental frequency responses presented in Figure 4 (b) show excellent agreement.



(a)



(b)

Figure 4 - Experimental output (Fs=15kHz).
(a) time response (β=21/64).
(b) Frequency responses,
..... -Theoretical and __-Experimental.

4 SECOND ORDER SECTION

As an application of the second generation SI integrator we built a biquadratic section, designed using backward LDI transformation (Silva-Martinez, 1989). This transformation leads to smaller frequency prewarping errors than the Euler transformations. The biquad circuit is presented in Figure 5. The center frequency ω_o and the quality factor Q can be controlled independently if the sampling frequency is much higher than the center frequency. In this case:

$$\omega_o T \cong a \tag{5.a}$$

and

$$Q \cong 1/f \tag{5.b}$$

A discrete prototype of the filter has been implemented and tested. In this experimental work, the transistors were replaced by resistors. The programmability of the filter was obtained by scaling the resistances. The unit resistor is 20kΩ, and the holding capacitors are C=100pF. The band pass filter has been programmed for center frequencies f_o=150, 300 and 600Hz. The sampling frequency was 15kHz and the quality factor was equal to 8. The simulation and experimental results are shown in Fig 6. In the case of very low $\omega_o T$, the error in the center frequency is large due to the variability of the resistors. To adjust this error we have to decrease the variability of the resistance or, for an IC implementation, increase the resolution of the MOCD.

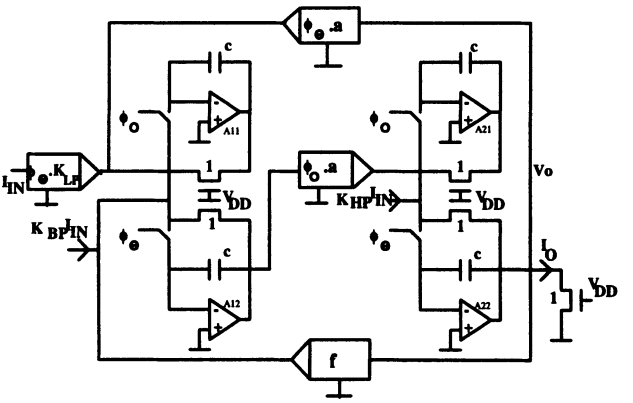


Figure 5 - Biquadratic section using second-generation SI integrator.

The DC output caused by the op amp offsets is

$$V_O = (1+G_{DC})V_{off1} + (2+\frac{1}{Q})\frac{\Delta V}{\omega_o T} \tag{6}$$

where G_{DC} is the low frequency gain (K_{LP}/a),

V_{off1} is the op amp (A_{11}) offset and
ΔV is the offset mismatch$\{V_{off1}(A_{11})-V_{off2}(A_{12})\}$.

The DC component of the output, as given by (6), is not large provided that the sampling frequency is not very much higher than the center frequency of the biquad or the offset mismatch is not high. Dynamic techniques (Vittoz, 1994) can also be employed to reduce the effects of the offset mismatch.

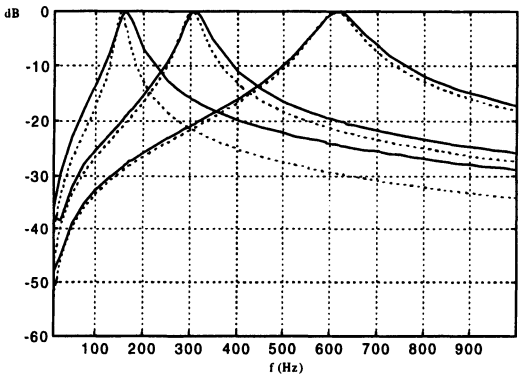


Figure 6 Magnitudes of the bandpass filter,
...-Theoretical and __-Experimental
f_0=150, 300 and 600 Hz (Q=8 and f_s=15kHz)

5 CONCLUSIONS

A second generation SI integrator has been reported in this work. The main advantage of the integrator presented here, when compared to the conventional one, is its applicability in low voltage circuits. Moreover, the constant voltage switching provides the circuit with a signal-independent charge injection. The programmability of the SI integrator has been tested using a digitally programmable MOCD. A bandpass SI filter has been implemented with discrete elements and tested at different center frequencies.

ACKNOWLEDGMENTS

The authors would like to thank the financial support of CNPq and CAPES, research/education agencies of the Brazilian Ministries of Science and Technology and Education.

6 REFERENCES

Bult, (1992) K. and Geelen, G. J. G. M. "An Inherently Linear and Compact MOST-Only Current Division Technique", IEEE J. Solid-State Circuits, vol. 27, no. 12, pp. 1730-1735, December 1992.

Crols, (1994) J. and Steyaert, M. "Switched-Opamp: An Approach to Realize Full CMOS Switched-Capacitor Circuits at Very Low Power Supply Voltages", IEEE J. Solid-State Circuits, vol. 29, no. 8, pp. 936-942, August 1994.

Fiez (1991) , T. S. Liang, G. and Allstot, D. "Switched-Current Circuit Design Issues "IEEE Journal of Solid State Circuits, Vol. 26, No. 3, pp. 192-202, March 1991.

Gonçalves, (1996 A) R. T. Noceti Filho, S. Schneider, M. C. and Galup-Montoro, C. "Digitally Programmable Switched Current Filters", in Proc. IEEE ISCAS, vol. 1, pp. 258-261, May 1996.

Gonçalves, (1996 B) R. T.and Galup-Montoro, C. "Analog Circuit on a Digital SOT Array", in Proc. of XI Conf. of Brazilian Microelectronics Society, Águas de Lindóia, SP, Brazil, pp 55- 60, August 1996.

Hughes, (1989) J. B. BirdN, C. and Macbeth, I. C. "Switched Currents - A New Technique for Analog Sampled-Data Signal Processing", in Proc. IEEE ISCAS, pp. 1584-1587, May 1989.

Hughes, (1990) J. B. Macbeth, I. C. and Pattullo, D. M. "Second Generation Switched-Current Signal Processing", in Proc. IEEE ISCAS., pp. 2805-2808, May 1990.

Queiroz, (1993) A. C. M. Pinheiro, P. R. M. and Calôba, L. P. "Nodal Analysis of Switched-Current Filters", IEEE Trans. on Circuit and System II, vol. 40, no. 1, pp. 10-18. January 1993.

Silva-Martinez, (1989) J. and Sánchez-Sinencio, E. "Biquadratic Programmable SC Filters with Additional Flexibility and Reduced Total Capacitance " Int. Journal of Circuit Theory and Applications, vol. 17, no. 2, pp. 241-248, April 1989.

Tsividis (1994), Y P. " Integrated Continuous-Time Filter Design - An Overview " IEEE Journal of Solid-State Circuits, Vol. 29, No. 3, pp. 166-176, March 1994.

Vittoz, (1994) E.A. "Micropower Techniques", in "Design of Digital VLSI Circuits for Telecommunications and Signal Processing " J.E. Franca and Y. P. Tsividis (Eds), Prentice Hall, 1994.

-Fathi A. F. FARAG was born in Egypt, on October 21, 1963, He received the B. S. and M. S. degree in electronic engineering from Assiut University, Assuit, Egypt, in 1986 and 1991 respectively. He is assistant lecture in electric Eng. Dept., Assuit university. Currently, he is working for the doctoral degree in the Electrical Engineering Dept., UFSC, Florianópolis-SC, Brazil.

His research interests includes sample data circuits (SC and SI) and Low voltage analog CMOS IC design.

-Renato Faustino was born in Garça, SP, Brazil on January 26, 1971. He Received the B. s. degree in electrical engineering from Escola de Engenharia de Lins, Lins, SP, Brazil, in 1993 and the M. S. Degree in Electric Engineering from Universdade Federal de Santa Catarina (UFSC), Florianólopis , SC,Brazil in 1996.

His research interests are integrated circuit and Digital filter design.

-Sidnei Noceti Filho was born in Florianópolis, SC, Brazil on December 17, 1952. He received the B. E. and M. S. degrees in electrical engineering from Unversidade Federal de Santa Catarina (UFSC), Florianópolis, SC, Brazil, in 1975 and 1980 respectively. He received the Doctoral degree in electrical engineering from Universidade Federal do Rio de Janeiro (COPPE/UFRJ), RJ,Brazil, in 1985.

In 1976 he joined the Electrical Engineering Department of UFSC where he has been engaged in education and research on signal processing and circuit analysis and design. He has been a professor in UFSC since 1993.

-Carlos. Galup-Montoro (M'89) was born in 1953 in Montevideo, Uruguay. He received the engineer degree in electronics from the Institute National Polytechnique de Grenoble (INPG), France, in 1979 and the doctor engineer degree in 1982 also from INPG.

Since 1990 he has been with the Electric Engineering Department at Unversidade Federal de Santa Catarina, Florianópolis, SC, Brazil, where he is now professor. His current research interests are device modeling and integrated circuits design.

-Marcio. C. Schneider received his B. S. E. E. and M. S. degrees from Federal University of Santa Catarina, Brazil, in 1975 and 1980 and the D. Eng. degree from University of Sao paulo, Brazil, in 1984. He is a professor at the Federal University of Santa Catarina. Currently he is a visiting professor at Texas A&M University. His interests are in the areas of Solid-State circuits and transistor modeling.