1

ASIC/System Hardware Verification at Nortel: A View from the Trenches

A. Silburt
Hardware System Modeling Group
Nortel Semiconductors
185 Corkstown Road
Nepean, Ontario K2H 8V4 Canada

Abstract

The emergence of functional verification as the largest single component of the ASIC development cycle has come as a bit of a surprise to the design community. At Nortel, we have had a group focusing on the methodologies used at this stage of the design for four years. Our involvement with some of the largest Nortel hardware designs has provided us with first-hand experience of the challenges in establishing confidence that ASICs will work the first time out in a system. This talk will describe the scope of the problems faced in ASIC-intensive telecomm systems, the methodologies currently deployed, and the emerging technologies that we are looking towards in the future to improve our ability to handle complex hardware systems.