A Pattern-Associative Router for Interconnection Network Adaptive Algorithms

Daniel G. Rice[1,2] Jose G. Delgado-Frias[1] and Douglas H. Summerville[1]

[1]Electrical Eng., SUNY, Binghamton, NY 13902 [2]Lockheed Martin, Owego, NY 13827

Abstract. In this paper, we propose a high-performance router approach to handle adaptive, deadlock-free, wormhole routing algorithms in a number of interconnection network topologies. The router allows programmable support for a wide range of networks and routing algorithms. Routing algorithms are mapped to a set of bit-patterns which are matched in parallel. The number of bit patterns required depends on the network topology and adaptive routing algorithm; in general this number is of O(network degree). To show the applicability of this adaptive router, we have studied a number of adaptive routing algorithms.

1 Introduction

A number of reconfigurable routers have been proposed to provide the flexibility to support various network topologies and routing algorithms. Two main approaches have been used: dedicated processors and look-up tables. The dedicated processor approach allows the router to perform with great flexibility the computations necessary to support multiple configurations of the network [7]. A drawback of this type of router is that the routing algorithm program must be executed in a sequential fashion. The look-up table approach requires that each routing alternative for any given destination address from a given node be stored in memory. The look-up table approach requires only one memory access delay to determine the output channel. However, large tables are required to store the routing information. Interval routing, a derivative of look-up table routing, assigns output ports to a range of destination node addresses, thus reducing the amount of memory required to store the look-up table [8]. This type of router might not be well suited to adaptive routing algorithms because the look-up table provides only one possible solution to the routing problem for a given set of inputs.

In this paper, we propose a new approach to adaptive routing algorithm execution. We will use wormhole routing algorithms in this paper as a means to introduce the approach; however the approach is applicable to any flow control technique. Our proposed router scheme provides the flexibility to support oblivious and adaptive routing algorithms for a variety of interconnection network topologies. The proposed router utilizes a pattern matching array that contains a relatively small number of bit patterns that are used to compare in parallel a number of potential routing alternatives. The adaptive router is composed of pattern match units to support routing, selection, and channel dependency enforcement functions. This approach allows the same scheme to be utilized for both oblivious and adaptive algorithms on a large number of interconnection networks.

2 Pattern-Associative Adaptive Router

An adaptive router approach uses two main functions, namely a routing function (R) and a selection function (ρ). The routing function defines a set of channels (physical/virtual channel pairs) that may be used for the current message. The selection function then determines which of these channels to use based on network status information (α_{pv}). This adaptive

router approach has been used by Dally and Aoki [1] and Duato [2]. Our proposed adaptive router approach separates the selection of physical channel from the selection of virtual channel, according to Theorem 1, below. This separation allows simplification of the routing and selection functions without sacrificing an algorithm's deadlock-freedom. A proof for this theorem is presented in [10].

Theorem 1: A connected and adaptive routing function R for an interconnection network I may be divided into selection of physical channel followed by enforcement of virtual channel dependencies without sacrificing deadlock-freedom.

The adaptive router proposed by Theorem 1 is shown in Figure 1. The three main functions are routing (R), selection (ρ), and dependency enforcement (E). The routing function (R) determines a set of alternative physical channels which may be used by the message to reach its destination. The selection function (ρ) then selects one of these physical channels from the alternatives presented. The dependency enforcement function (E) ensures that the proper virtual channel is used to meet the requirements of the channel dependency graph for the routing algorithm. The proposed adaptive router approach divides the adaptive routing problem into smaller subtasks. First, a set of valid alternative physical channels are determined. Second, the best physical channel is chosen from this set of alternatives based on information about these channels. Finally, a valid virtual channel is determined for the physical channel selected, and the message is routed on the resulting physical channel/virtual channel pair. Adaptive routing algorithms that can be partitioned into physical and virtual channels should not be affected by the proposed adaptive router scheme.

The proposed adaptive router scheme offers four major advantages over the basic router. These advantages are: *small subtasks*, the approach divides the routing function into smaller subtasks, which can be optimized to reduce the number of bit-pattern entries; *small set of alternative physical paths*, the routing function determines alternative physical channels from the domain of physical channels available; *simpler selection function*, the selection function is simplified by reducing the domain of possible inputs; and *simplified dependency enforcement*, the dependency enforcement function can be optimized for the particular routing algorithm to be implemented.

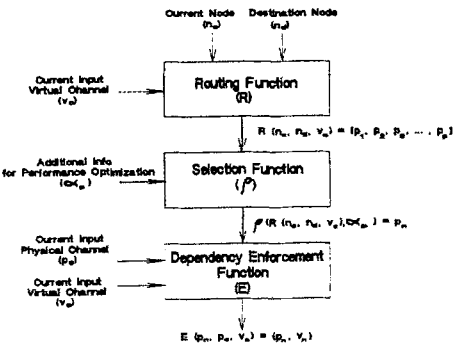

Figure 1. Proposed Adaptive Router Scheme

The bit-pattern associative router relies on network topological information inherent in the network addressing scheme. The router uses sets of bits from the destination node address to determine an output port assignment for the current message. For adaptive algorithms, the router allows multiple paths to be considered, and selects the "best" path based on network status information available to the router. The router's basic constructs allow implementation of a large number of oblivious and adaptive routing algorithms for a large variety of interconnection networks. A block diagram representation of the bit pattern matching unit scheme is shown in Figure 2(a). The bit pattern match section utilizes a matching mechanism which allows multiple bit-pattern alternatives to be considered in parallel and each viable alternative is presented to the priority selection section. [6] The matching unit allows "don't care" bits to used as part of the patterns to be tested, to reduce the number of patterns required in the array. This technique allows only those bits which are important to the routing decision to be considered for each routing alternative. The priority selection section selects a single alternative from the bit pattern match "hits" based on a fixed priority scheme. The port assignment memory contains physical or virtual port assignments for each bit pattern match.

The three main functions (routing, selection and dependency enforcement) of this approach are implemented using two pattern matching units as shown in Figure 2(b). The first pattern matching unit performs the routing and selection functions, and the second matching unit performs the dependency enforcement function. Each pattern matching unit consists of a bit pattern match section, a priority selector section, and a port assignment memory. The routing function uses the destination address from the message header, and the "free/busy" bits for the corresponding physical output ports. This approach is well-suited to use a single "free/busy" bit for each output port, although more complex channel status reporting mechanisms are possible. The selection function chooses the most attractive output port from the options available. For general adaptive algorithm implementations, a miscellaneous output port assignment field is provided in addition to the physical channel output port field. This miscellaneous field allows simpler implementation of some adaptive routing algorithms. Both the selected physical channel port and the miscellaneous field data are passed to the dependency enforcement matching unit (virtual channel selection). The dependency enforcement function also uses a pattern matching unit. The bit pattern fields that are used to determine which virtual channel will be utilized are the selected physical channel, the virtual channel status for the selected physical channel, and in some instances, the

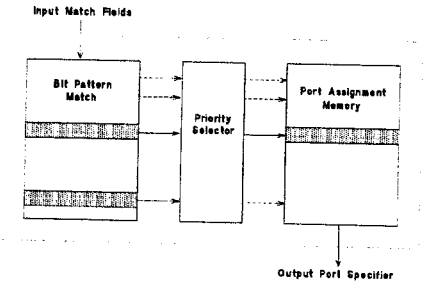

Figure 2(a). Bit Pattern Matching Unit Block Diagram

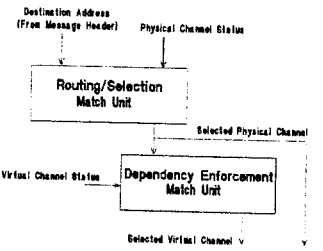

Figure 2(b). Proposed Adaptive Router Approach

miscellaneous field from the router/physical channel selection function, or the current input physical and virtual channels for the message. The output port memory for the dependency enforcement matching unit contains virtual channel alternatives for the selected physical channel.

3 Mapping of Adaptive Routing Algorithms to Proposed Scheme

We have chosen an example algorithm to demonstrate the bit-pattern associative router concept. Our example is a deadlock-free static dimension-reversal algorithm for mesh-connected k-ary n-cube networks [1] applied to the hypercube. This adaptive algorithm utilizes a count of the number of times a packet has been routed from a channel in one dimension to channel in a lower dimension (the dimension-reversal or DR number) to select the virtual channel to be used for routing to avoid deadlock. Each physical channel is divided into non-empty classes of virtual channels numbered zero to r, where r is the maximum number of dimension reversals permitted. Packets with DR < r may be routed in any direction, but must use virtual channels of class DR. Once a packet's DR = r, it must be routed in ascending dimension order towards its destination, and may not re-enter the adaptive channels. The bit patterns for this algorithm are shown in Figure 3.

The selection function for the algorithm chooses an unoccupied, productive channel if possible. Only when no adaptive channels are available (ie. packet DR = r) does the packet resort to deterministic dimension-order routing. The selection function may utilize a variety of schemes to select the output channel from those available.

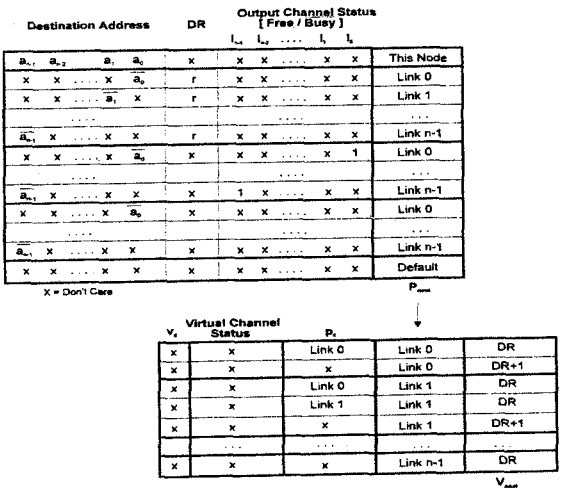

Figure 3. Bit Pattern Mapping for Static Dimension Reversal Algorithm

4 Concluding Remarks

The proposed scheme to adaptive routing presented in this paper is applicable to a wide range of interconnection networks and adaptive routing algorithms. The mapping of some of these algorithms have been provided to demonstrate the applicability of this approach. Additional adaptive routing algorithms including the Fully Adaptive Algorithm [2,5], Planar Adaptive Routing (PAR) [3], Linder and Harden's virtual networks concepts [4] and turn-model based algorithms [9] have been mapped to this approach. The adaptive router uses a novel bit-pattern match unit to create a flexible router for a variety of network implementations and routing algorithms. The performance of the pattern-associative adaptive router is based on the performance of each of the two stages of the router. If no stage pipelining is used, a total of two comparison delays and two read delays are needed for the full adaptive router. Compared to other flexible adaptive router schemes, the proposed bit-pattern adaptive router is a high-performance approach. The adaptive router can be utilized with no changes to hardware or bit patterns as the network expands, so long as sufficient address bits are included in the initial implementation to support the additional node addresses.

References

[1] W. Dally and H. Aoki, "Deadlock-free adaptive routing in multicomputer networks using virtual channels," *IEEE Trans. Parallel Dist. Syst.*, vol. 4, no. 4, Apr. 1993, pp. 466- 475.

[2] J. Duato, "A new theory of deadlock-free adaptive routing in wormhole networks," *IEEE Trans. Parallel Dist. Syst.*, vol. 4, no. 12, Dec. 1993, pp. 1320-1331.

[3] J. Kim and A. Chien, "An evaluation of planar adaptive routing (PAR)", *Proc. 4th IEEE Symp. Parallel Distrib. Processing*, Dec. 1992, pp. 470-478.

[4] D. Linder and J. Harden, "An adaptive and fault tolerant wormhole routing strategy for k-ary n-cubes," *IEEE Trans. Comput.*, vol. 40, no. 1, Jan. 1991, pp. 2-12.

[5] J. Duato, "Deadlock-free adaptive routing algorithms for multicomputers: Evaluation of a new algorithm," *Proc. 3rd IEEE Symp. Parallel Distrib. Processing*, 1991, pp. 840-847.

[6] D. Summerville, J. Delgado-Frias and S. Vassiliadis, "A flexible bit-associative router for interconnection networks," *IEEE Trans. Parallel Dist. Syst.*, vol. 6, no. 5, May 1996.

[7] J. Park, S. Vassiliadis, and J.G. Delgado-Frias, "Flexible oblivious router architecture," *IBM Journal of Research and Development*, vol. 39, no. 3, pp. 315-329, May 1995.

[8] J. Van Leeuwen and R.B. Tan, "Interval routing," *The Computer Journal*, vol. 30, no. 4, pp. 298-307, 1987.

[9] C.J. Glass and L.M. Ni, "The turn model for adaptive routing," *Journal of the ACM*, vol. 41, no. 5, pp. 874-902, Sept. 1994.

[10] D.G. Rice, J.G. Delgado-Frias and D.H. Summerville, "A Pattern-Associate Router for Adaptive Algorithms in Hypercube Networks," *IASTED Int. Conf. Parallel and Dist. Systems*,Washington, DC, October, 1995.