Turn-Regularity and Planar Orthogonal Drawings[*]
(Extended Abstract)

Stina S. Bridgeman[1], Giuseppe Di Battista[2], Walter Didimo[2],
Giuseppe Liotta[3], Roberto Tamassia[1], and Luca Vismara[1]

[1] Center for Geometric Computing, Department of Computer Science,
Brown University, 115 Waterman Street, Providence, RI 02912–1910.
`{ssb,rt,lv}@cs.brown.edu`
[2] Dipartimento di Informatica e Automazione,
Università degli Studi di Roma Tre, Via della Vasca Navale 79, 00146 Roma, Italy.
`{gdb,didimo}@dia.uniroma3.it`
[3] Dipartimento di Ingegneria Elettronica e dell'Informazione,
Università degli Studi di Perugia, Via Duranti 93, 06131 Perugia, Italy.
`liotta@diei.unipg.it`

Abstract. Given an orthogonal representation H with n vertices and
bends, we study the problem of computing a planar orthogonal dra-
wing of H with small area. This problem has direct applications to the
development of practical graph drawing techniques for information vi-
sualization and VLSI layout. In this paper, we introduce the concept of
turn-regularity of an orthogonal representation H, provide combinato-
rial characterizations of it, and show that if H is turn-regular (i.e., all
its faces are turn-regular), then a planar orthogonal drawing of H with
minimum area can be computed in $O(n)$ time, and a planar orthogo-
nal drawing of H with minimum area and minimum total edge length
within that area can be computed in $O(n^{7/4} \log n)$ time. We also apply
our theoretical results to the design and implementation of new practical
heuristic methods for constructing planar orthogonal drawings. An ex-
perimental study conducted on a test suite of orthogonal representations
of randomly generated biconnected 4-planar graphs shows that the per-
centage of turn-regular faces is quite high and that our heuristic drawing
methods perform better than previous ones.

1 Introduction

Orthogonal drawings are drawings of graphs in which every edge is represented
by a chain of horizontal and vertical segments. An orthogonal representation is
an equivalence class of orthogonal drawings that have the same "shape" (see

Fig. 1). This class is formally described by specifying the bends along each edge and the angles between consecutive edges around each vertex. In this paper we consider planar orthogonal representations, that is, equivalence classes of orthogonal drawings for which at least one of the drawings is planar. Given a planar orthogonal representation H, the problem of finding a planar orthogonal grid drawing of H with small area is usually referred to as the *compaction* of H.

Orthogonal representations and planar orthogonal drawings have been extensively investigated (see, e.g., [1, 9, 11, 12, 14, 15, 16, 18, 27, 28, 29, 30]) because of their direct applications to the development of practical graph drawing techniques for information visualization [6]. In particular, it has been experimentally shown that drawing algorithms for general graphs based on the compaction of orthogonal representations with minimum number of bends perform better in practice than other known orthogonal drawing algorithms [7, 25]. Orthogonal representations and related concepts, such as slicing floorplans, are also widely used in VLSI layout compaction algorithms (see, e.g., [19, 21, 22, 26, 31]).
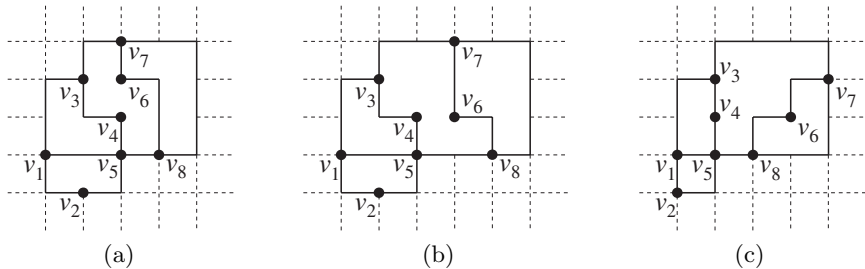

Fig. 1. Three planar orthogonal drawings of a graph. Two drawings of the same orthogonal representation are shown in (a) and (b), while a drawing of a different orthogonal representation is shown in (c). The drawing in (a) has optimal area among all planar drawings of that orthogonal representation.

Despite the significant body of research on orthogonal representations, the development of effective compaction techniques remains a challenging task. It has been conjectured for a long time [30], and recently proved [24], that the optimal compaction of planar orthogonal representations, i.e., computing a minimum area planar orthogonal grid drawing of a given planar orthogonal representation, is an NP-complete problem. The only class of planar orthogonal representations for which a polynomial-time optimal compaction algorithm is known is the trivial class of orthogonal representations whose faces are all rectangular [6].

From a practical perspective, the compaction algorithms used by current graph drawing libraries and systems, such as AGD[1], $GDToolkit$[2], and the *Graph Drawing Server*[3], are all variations of the compaction technique presented in [18,

27], which is based on the idea of splitting faces into rectangles. Since the splitting imposes unnecessary constraints on the geometry, the resulting drawings may have substantially suboptimal area.

The importance of compaction techniques for graph visualization applications is confirmed by a recent work of Klau and Mutzel [20]. They consider the problem of assigning coordinates to vertices and edge bends of an orthogonal representation so that the total edge length is minimized. The problem is formulated as an integer linear program, whose practical performance is fairly good. Also, they show that the problem can be solved in polynomial time for those orthogonal representations in which there is only one possible relative position of any two vertices that results in a planar drawing; in this case, the inequalities of the corresponding ILP formulation form a totally unimodular matrix. The problem of minimizing the area of the drawing is not considered.

The main results of this paper can be summarized as follows.

- Given a planar orthogonal representation H, we define the concept of *turn-regularity* of a face of H, which is based on the structure of the sequence of left and right turns encountered when traversing the face. We show that the turn-regularity of a face can be tested in linear time.
- We relate turn-regularity to the concept of *switch-regularity* [8]. Namely, we characterize the turn-regularity of a face f in terms of the switch-regularity of two upward orientations of f.
- We introduce the concept of *orthogonal relation* between two vertices of H. This relation establishes the relative position of the two vertices in any planar orthogonal drawing of H. We show that an orthogonal relation is defined between every two vertices of H if and only if all the faces of H are turn-regular.
- We show that if H is turn-regular (i.e., all its faces are turn-regular), then any orthogonal drawing of H such that the orthogonal relations between every two vertices are satisfied is planar.
- We show that if H is turn-regular, then a planar orthogonal drawing of H with optimal area can be computed in $O(n)$ time and space, where n is the number of vertices and bends of H. Furthermore, a planar orthogonal drawing of H with optimal area and minimum total edge length within that area can be computed in $O(n^{7/4} \log n)$ time.
- We present the results of an experimental study on a test suite of planar orthogonal representations of randomly generated biconnected 4-planar graphs. The experiments show that the percentage of turn-regular faces is quite high (the average value is 89%). Motivated by this result, we have designed compaction heuristics based on the idea of "face turn-regularization". Namely, we decompose non-turn-regular faces into turn-regular ones, and then perform an optimal compaction of the resulting planar orthogonal representation. We implemented our compaction algorithms and experimentally observed that the improvement in area is substantial when compared to the compaction algorithms available in state-of-the-art graph drawing libraries.

Due to space limitations, some technical lemmas, the proofs, and some figures are omitted in this extended abstract. A full version of this paper is available on-line at `ftp://ftp.cs.brown.edu/pub/techreports/99/cs99-04.ps.Z`.

2   Preliminaries

2.1   Basic Definitions

We assume familiarity with graph terminology and basic properties of planar graphs (see, e.g., [5, 17]). The graphs we consider are assumed to be connected. For background on graph drawing, see [6].

An *st-digraph* is an acyclic digraph with a single source s (vertex with no incoming edges) and a single sink t (vertex with no outgoing edges). A *planar st-digraph* is an st-digraph that is planar and embedded with vertices s and t on the boundary of the external face. An important property of planar st-digraphs is that the incoming edges of each vertex v appear consecutively around v, as do the outgoing edges. Also, the boundary of each face f consists of two directed paths enclosing f, with common origin and destination.

A planar graph whose vertices have degree at most four is said to be 4-*planar*. Let G be an embedded 4-planar graph and let f be a face of G. In the following, we always traverse the boundary of f so that f is on the left, i.e., counterclockwise if f is internal and clockwise if f is external. The boundary of f consists of an alternating circular sequence of vertices and edges. Note that if G is not biconnected, there may be two occurrences of the same edge and multiple occurrences of the same vertex on the boundary of f. We denote by a_f the number of vertices (or edges) of f, each counted with its multiplicity.

Informally speaking, an *orthogonal representation* of an embedded 4-planar graph G describes an equivalence class of orthogonal drawings of G with "similar shape". It consists of a "decorated" version of G where each pair of consecutive edges around a vertex v is assigned an angle multiple of $\pi/2$ and each edge (u, v) is assigned a sequence of bends going from u to v, each a left or right turn. In this paper we consider *planar orthogonal representations*, that is, equivalence classes of orthogonal drawings for which at least one of the drawings is planar; in the rest of the paper, we omit the word planar when referring to orthogonal representations. For a detailed definition of orthogonal representation, see, e.g., [6].

Since each bend can be replaced by a dummy vertex of degree 2, in the rest of the paper we assume, for the sake of simplicity, that orthogonal representations have no bends. We also assume that different drawings of the same orthogonal representation are iso-oriented, i.e., each edge has the same direction and its end-vertices are in the same relative position.

2.2   Switch-Regularity

We recall some terminology and results from [2, 8, 10]. A drawing of a digraph is said to be *upward* if edges are mapped to curves monotonically increasing in a

common direction, for instance the vertical one. A digraph is *upward planar* if it admits an upward planar drawing. As we are going to show in the next section, upward planar drawings and orthogonal representations are strictly related. We recall here some notations and results that will be useful in the rest of the paper.

A vertex v of an embedded planar digraph G is said to be *bimodal* if all the incoming edges of v appear consecutively around it in the embedding, and so do the outgoing edges. If all the vertices of G are bimodal then G and its embedding are called *bimodal*. Let f be a face of a bimodal embedded planar digraph G. A vertex v of f with incident edges e_1 and e_2 on the boundary of f is a *switch* of f if e_1 and e_2 are both incoming or both outgoing edges (note that e_1 and e_2 may coincide if the digraph is not biconnected). In the former case v is a *sink-switch* of f, in the latter a *source-switch* of f. Observe that a source (sink) of G is a source-switch (sink-switch) of all its incident faces; a vertex of G that is not a source or a sink is a switch of all its incident faces except two. We denote by $2n_f$ the number of switches of f.

Assign S and L labels to the switches of each face of a bimodal embedded planar digraph G such that (see Fig. 2a): (i) each source or sink of G has exactly one L label; (ii) for each face f, the number of L-labeled switches assigned to f is equal to $n_f - 1$ if f is an internal face, and to $n_f + 1$ if f is the external face. The S-labeled (L-labeled) source-switches are called s_S-switches (s_L-switches) and the S-labeled (L-labeled) sink-switches are called t_S-switches (t_L-switches). The circular sequence of labels of f so obtained is a *labeling* of f and is denoted by σ_f. Also, S_{σ_f} (L_{σ_f}) denotes the number of S-labels (L-labels) of σ_f. A face f of G labeled in this manner is *upward consistent*.
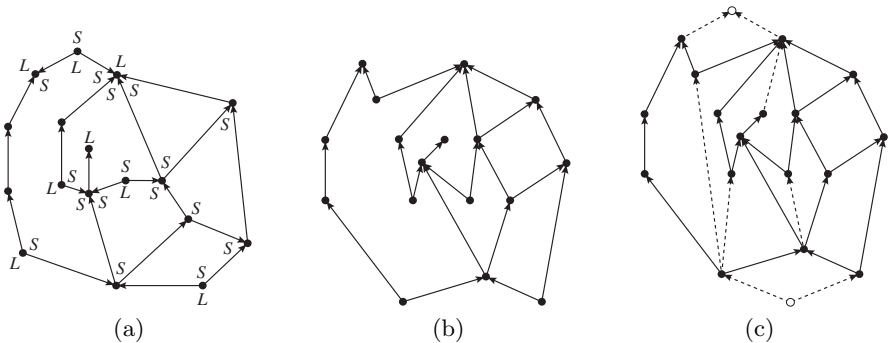

Fig. 2. (a) A bimodal embedded planar digraph G with an upward consistent labeling of its faces. (b) An upward planar drawing of G corresponding to the upward consistent labeling in (a). (c) A complete saturator of G; s and t are represented as white circles, and saturating edges are represented as dashed segments.

Theorem 1. [2] *A bimodal embedded digraph is upward planar if and only if all its faces have an upward consistent labeling.*

Let G be a bimodal embedded digraph such that all its faces have an upward consistent labeling. For each face of G, the S-label (L-label) assigned to a switch intuitively indicates that the angle formed by the two edges identifying the switch is smaller (larger) than π in an upward planar drawing of G. Any such drawing is said to *correspond* to the upward consistent labeling of the faces of G. On the other hand, given an upward planar drawing of a bimodal embedded digraph G, an upward consistent labeling for each face of G can be obtained by simply checking whether the angle formed by each pair of edges identifying a switch is smaller or larger than π. Figure 2b shows an upward planar drawing (corresponding to the upward consistent labeling) of the embedded planar digraph in Fig. 2a.

Given an embedded upward planar digraph G, a *saturator* of G is a set of vertices and edges, not belonging to G, with which we augment G. More precisely, a saturator consists of two vertices s and t, edge (s, t), and a set of edges (u, v) (each edge a *saturating edge*) such that:

- Vertices u and v are switches of the same face, or $u = s$ and v is an s_L-switch of the external face, or u is a t_L-switch of the external face and $v = t$.
- If, $u, v \neq s, t$, either u is an s_S-switch and v is an s_L-switch or u is a t_L-switch and v is a t_S-switch. In the former case we say that u *saturates* v and in the latter case we say that v *saturates* u.
- The faces obtained with the insertion of a saturating edge are upward consistent.

A saturator of G is said to be *complete* if for every face f and for every switch u of f labeled L, u is an end-vertex of an edge of the saturator (see Fig. 2c). Clearly, adding to G a complete saturator yields a planar st-digraph.

Lemma 1. [8] *Every upward planar embedding admits a complete saturator.*

An upward planar embedding may have, in general, several complete saturators. The class of embedded upward planar digraphs for which there exists a unique complete saturator has been characterized in [8]. The characterization is based on a certain type of labeling. Namely, let G be an embedded upward planar digraph. An internal face f of G has a *switch-regular labeling* if σ_f does not contain two distinct maximal subsequences σ_1 and σ_2 of S-labels such that $S_{\sigma_1} > 1$ and $S_{\sigma_2} > 1$. An external face f of G has a switch-regular labeling if σ_f does not contain two consecutive S-labels. (Note that a switch-regular labeling is called just regular labeling in [8].) A face of G with a switch-regular labeling is a *switch-regular* face. For example all faces of Fig. 2a are switch-regular. An embedded upward planar digraph is *switch-regular* if all its faces have a switch-regular labeling. The corresponding embedding is also called *switch-regular*.

Theorem 2. [8] *An upward planar embedding has a unique complete saturator if and only if it is switch-regular.*

3   Turn-Regularity and Switch-Regularity

3.1   Orthogonal Relations

Let G be an embedded 4-planar graph, H be an orthogonal representation of G, Γ be a planar drawing of H, and v be a vertex of G. We denote by $x(v)$ and $y(v)$ the x- and y-coordinates of the point representing v in Γ. We define four binary relations on the vertex set of G: for each pair $\{u, v\}$ of vertices of G, these relations determine the relative position of u and v in *all planar drawings* of H.

- $u <_x v$ if $x(u) < x(v)$ for all planar drawings of H; in this case, we say that u is *left* of v and that v is *right* of u.
- $u =_x v$ if $x(u) = x(v)$ for all planar drawings of H; in this case, we say that u is *x-aligned* with v.
- $u <_y v$ if $y(u) < y(v)$ for all planar drawings of H; in this case, we say that u is *below* v and that v is *above* u.
- $u =_y v$ if $y(u) = y(v)$ for all planar drawings of H; in this case, we say that u is *y-aligned* with v.

We refer to the first two binary relations as x-relations and to the second two binary relations as y-relations. As an example, in the orthogonal representation in Fig. 1 $v_2 <_x v_8$, $v_6 =_x v_7$, $v_2 <_y v_3$, and $v_1 =_y v_5$.

We define three new binary relations on the vertex set of G, obtained by combining an x-relation and a y-relation: $=_x \wedge <_y$, $<_x \wedge =_y$, and $<_x \wedge <_y$. These three binary relations together with the binary relations $<_x$ and $<_y$ are collectively referred to as *orthogonal relations*. As an example, in the orthogonal representation in Fig. 1 $v_5 =_x v_4 \wedge v_5 <_y v_4$, $v_1 <_x v_8 \wedge v_1 =_y v_8$, and $v_1 <_x v_7 \wedge v_1 <_y v_7$, while no orthogonal relation holds for $\{v_4, v_6\}$.

3.2   Turn-Regularity

To characterize those orthogonal representations that have an orthogonal relation for each pair of vertices, we introduce the notion of *turn-regularity*.

Let G be an embedded 4-planar graph, H be an orthogonal representation of G, and f be a face of G. For each occurrence of vertex v on the boundary of f, let $prev(v)$ and $next(v)$ be the edges preceding and following v, respectively, on the boundary of f. Note that $prev(v)$ and $next(v)$ may coincide if the graph is not biconnected. We associate with each occurrence of v one or two *corners*. Namely:

- If the angle internal to f between $prev(v)$ and $next(v)$ is $\pi/2$ in H, we associate with v one *convex* corner, and say that v corresponds to a *left turn*.
- If the angle internal to f between $prev(v)$ and $next(v)$ is π in H, we associate with v one *flat* corner, and say that v corresponds to a *flat turn*.
- If the angle internal to f between $prev(v)$ and $next(v)$ is $3\pi/2$ in H, we associate with v one *reflex* corner, and say that v corresponds to a *right turn*.

– If the angle internal to f between $prev(v)$ and $next(v)$ is 2π in H, we associate with v an ordered pair of *reflex* corners, and say that v corresponds to a *U-turn*.

Hence, a circular sequence of corners can be associated with the boundary of f. For each corner c of f, let $turn(c) = 1$ if c is convex, $turn(c) = 0$ if c is flat, and $turn(c) = -1$ if c is reflex. As an example, in Fig. 3 a convex corner is associated with v_1, a flat corner with v_2, a reflex corner with v_3, and an ordered pair of reflex corners with v_4. The grey portion of Fig. 3 represents the rest of the graph.
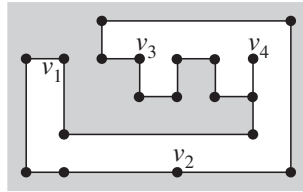
Fig. 3. A face of an orthogonal representation. The grey portion represents the rest of the graph.

For each ordered pair $\{c_i, c_j\}$ of corners associated with vertices of f, let $rotation(c_i, c_j) = \sum_c turn(c)$ for all corners c along the boundary of f from c_i (included) to c_j (excluded). If c_i and c_j are associated with distinct vertices v_i and v_j, respectively, $rotation(c_i, c_j) \cdot \pi/2$ is the net angle turned between $prev(v_i)$ and $prev(v_j)$. As an example, in Fig. 3 let c_1, c_2, and c_3 be the corners associated with v_1, v_2, and v_3, respectively, and let $\{c_4', c_4''\}$ be the ordered pair of corners associated with v_4; $rotation(c_1, c_2) = 3$, $rotation(c_3, c_4') = 1$, $rotation(c_3, c_4'') = 0$, and $rotation(c_3, c_1) = -3$.

Two reflex corners c_i and c_j are called *kitty corners* if $rotation(c_i, c_j) = 2$ or $rotation(c_j, c_i) = 2$. In Fig. 1, the corners associated with vertices v_4 and v_6 are kitty corners. A face of an orthogonal representation is *turn-regular* if it has no kitty corners. As an example, the face shown in Fig. 3 is turn-regular. An orthogonal representation is *turn-regular* if all its faces are turn-regular.

3.3   Turn-Regularity and Switch-Regularity

Let G be an embedded 4-planar graph, H be an orthogonal representation of G, and Γ be a planar drawing of H. Let Γ_r be an orientation of Γ such that all vertical segments are directed upward and all horizontal segments are directed rightward, and let Γ_ℓ be an orientation of Γ such that all vertical segments are directed upward and all horizontal segments are directed leftward. Observe that Γ_r is an upward planar drawing in the North-East direction and that Γ_ℓ is an upward planar drawing in the North-West direction. Γ_r and Γ_ℓ induce two orientations on H. We denote the oriented orthogonal representations by

H_r and H_ℓ. In turn, H_r and H_ℓ induce two orientations on G. We denote the embedded 4-planar digraphs by G_r^H and G_ℓ^H, respectively. Observe that G_r^H and G_ℓ^H are embedded upward planar digraphs. Also, note that different orthogonal representations of G induce, in general, different orientations on G; since we work with a fixed orthogonal representation of a graph, we use G_r and G_ℓ in the rest of the paper, omitting the reference to H.

Theorem 3. *An orthogonal representation H of an embedded 4-planar graph G is turn-regular if and only if the embedded upward planar digraphs G_r and G_ℓ are both switch-regular.*
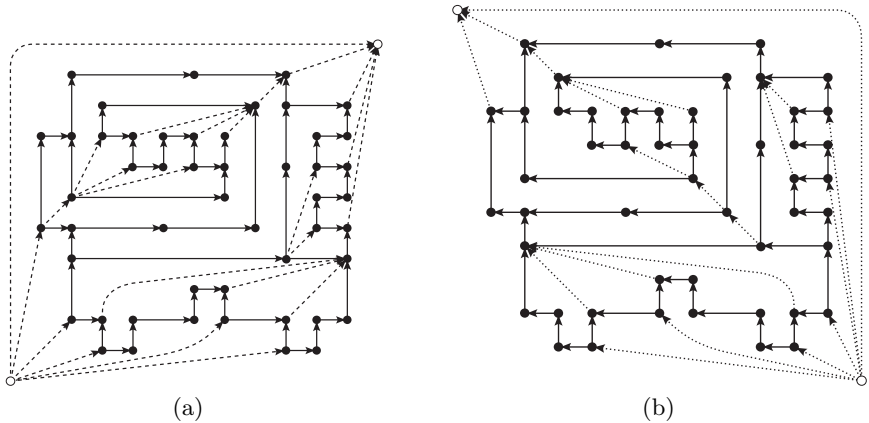
Fig. 4. (a) G_r (edges represented as solid segments) and a complete saturator (edges represented as dashed segments). (b) G_ℓ (edges represented as solid segments) and a complete saturator (edges represented as dotted segments).

4   Orientations and Paths

Let G be an embedded 4-planar graph and H be a turn-regular orthogonal representation of G. As seen in Section 2.2, a complete saturator of an embedded upward planar digraph consists of two vertices s and t and a set of (directed) saturating edges. Figure 4a shows a complete saturator of graph G_r corresponding to the oriented orthogonal representation H_r. Figure 4b shows a complete saturator of graph G_ℓ corresponding to the oriented orthogonal representation H_ℓ. In the rest of the paper we never consider the saturating edges of G_r and G_ℓ incident with s or t, even when not explicitly stated. Let f be an internal face of H; a maximal vertical or horizontal chain of f is said to be *unconstrained* if both its end-vertices correspond to a right turn of f. Note that an unconstrained maximal chain of f may consist of a single, degree one vertex.

We now construct two partially-directed graphs, one representing the "left" relation between maximal vertical chains of H, the other representing the "below" relation between maximal horizontal chains of H. The graph representing the "left" relation between maximal vertical chains of H is constructed as follows. We first augment H with the saturating edges of G_r and G_ℓ incident with an end-vertex of an unconstrained maximal vertical chain of H. We then orient the horizontal edges of H from left to right, reverse the orientation of the saturating edges of G_ℓ, and leave the vertical edges of H not oriented so that they can be traversed in both ways. We denote by H_x the resulting graph (see Fig. 5a). Similarly, the graph representing the "below" relation between maximal horizontal chains of H is constructed as follows. We first augment H with the saturating edges of G_r and G_ℓ incident with an end-vertex of an unconstrained maximal horizontal chain of H. We then orient the vertical edges of H from bottom to top and leave the horizontal edges of H not oriented so that they can be traversed in both ways. We denote by H_y the resulting graph (see Fig. 5b).
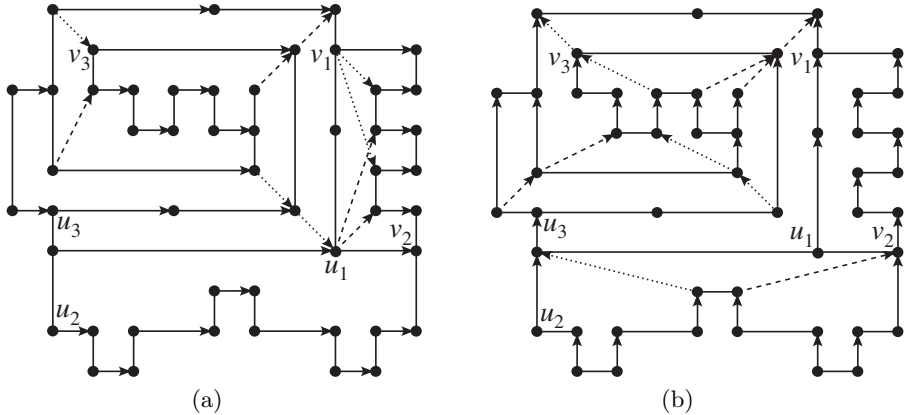

Fig. 5. (a) H_x. (b) H_y. Both graphs are obtained using the complete saturators shown in Fig. 4.

The following theorem shows how turn-regularity characterizes those orthogonal representations for which the "left" relation between maximal vertical chains and the "below" relation between maximal horizontal chains are uniquely determined.

Theorem 4. *Let H be an orthogonal representation of an embedded 4-planar graph. H_x and H_y are uniquely determined if and only if H is turn-regular.*

Note that H_x and H_y are no longer orthogonal representations, and may, in general, be non-planar. From the definition of saturator, it follows that each saturating edge from G_r and G_ℓ used in the construction of H_x and H_y has both end-vertices on the same face of H. Two saturating edges in H_x or H_y are said

to *cross* each other if their end-vertices appear alternately on the boundary of a common face of H. In the rest of the paper we refer to the maximal chains of non-oriented edges of H_x as maximal vertical chains of H_x, and denote by $mvc(v)$ the maximal vertical chain of H_x containing vertex v. Analogously, we refer to the maximal chains of non-oriented edges of H_y as maximal horizontal chains of H_y, and denote by $mhc(v)$ the maximal horizontal chain of H_y containing vertex v.

5   Turn-Regularity and Orthogonal Relations

In this section we use graphs H_x and H_y to characterize all possible orthogonal relations in a turn-regular orthogonal representation. This leads to a characterization of turn-regular orthogonal representations in terms of orthogonal relations. We denote by $u \to v$ a directed path from vertex u to vertex v in H_x containing at least a horizontal edge or in H_y containing at least a vertical edge, and by $u \nrightarrow v$ the absence of such a path from vertex u to vertex v.

Lemma 2. *For each pair $\{u, v\}$ of vertices of H_x the following conditions hold:*

1. *$mvc(u) = mvc(v)$ if and only if $u =_x v$*
2. *$u \to v$ if and only if $u <_x v$*
3. *$v \to u$ if and only if $v <_x u$*
4. *$mvc(u) \neq mvc(v)$, $u \nrightarrow v$, and $v \nrightarrow u$ if and only if no x-relation can be established between u and v.*

As an example, we identify in the graph H_x shown in Fig. 5a three pairs of vertices corresponding to the various cases of Lemma 2: u_1 and v_1 belong to the same maximal vertical chain, there exists a directed path from u_2 to v_2, while there is neither a path between u_3 and v_3, nor they belong to the same maximal vertical chain.

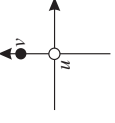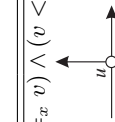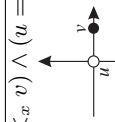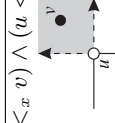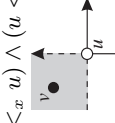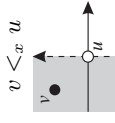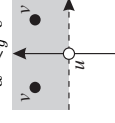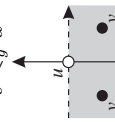**Lemma 3.** *For each pair $\{u, v\}$ of vertices of H_y the following conditions hold:*
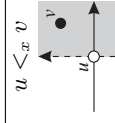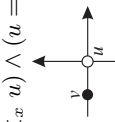
1. *$mhc(u) = mhc(v)$ if and only if $u =_y v$*
2. *$u \to v$ if and only if $u <_y v$*
3. *$v \to u$ if and only if $v <_y u$*
4. *$mhc(u) \neq mhc(v)$, $u \nrightarrow v$, and $v \nrightarrow u$ if and only if no y-relation can be established between u and v.*

Lemma 4. *Let G be an embedded 4-planar graph and H be a turn-regular orthogonal representation of G. For each pair $\{u, v\}$ of vertices of G, exactly one orthogonal relation holds (see Table 1).*

We are interested in those orthogonal representations for which there is an orthogonal relation between each pair of vertices. As the following theorem shows, this class of orthogonal representations is characterized by turn-regularity.

Theorem 5. *An orthogonal representation H of an embedded 4-planar graph is turn-regular if and only if there is an orthogonal relation between every two vertices of H.*

Table 1. Orthogonal relations for a pair $\{u, v\}$ of vertices in a turn-regular orthogonal representation H.

H_x \ H_y	$mhc(u) = mhc(v)$	$u \to v$	$v \to u$	otherwise
$mvc(u) = mvc(v)$	impossible	$(u =_x v) \wedge (u <_y v)$	$(u =_x v) \wedge (v <_y u)$	impossible
$u \to v$	$(u <_x v) \wedge (u =_y v)$	$(u <_x v) \wedge (u <_y v)$	$(u <_x v) \wedge (v <_y u)$	$u <_x v$
$v \to u$	$(v <_x u) \wedge (u =_y v)$	$(v <_x u) \wedge (u <_y v)$	$(v <_x u) \wedge (v <_y u)$	$v <_x u$
otherwise	impossible	$u <_y v$	$v <_y u$	impossible

6   Turn-Regularity and Drawing Algorithms

In this section we first study the problem of efficiently checking whether an orthogonal representation is turn-regular. Then we show how an optimal area orthogonal drawing of a turn-regular orthogonal representation can be computed.

Theorem 6. *A turn-regular orthogonal representation of an embedded 4-planar graph with n vertices and bends can be recognized in $O(n)$ time and space.*

The optimal area drawings that we want to compute are planar. The next theorem guarantees the planarity of drawings that satisfy the orthogonal relations of a turn-regular orthogonal representation.

Theorem 7. *Let H be a turn-regular orthogonal representation of an embedded 4-planar graph, and let Γ be an orthogonal drawing of H such that, for each pair $\{u, v\}$ of vertices of H, the orthogonal relation between u and v is satisfied. Then Γ is planar.*

We are now ready to present two different algorithms that compute optimal area drawings of turn-regular orthogonal representations. These algorithms are variations of the two compaction procedures described in [6]. For the first algorithm, we define two digraphs, denoted D_x and D_y. D_x is obtained from H_x by shrinking each maximal vertical chain to a single vertex, by removing possible multiple edges, and by adding a super-source and a super-sink (see Fig 6a). Thus, there is a one-to-one correspondence between maximal vertical chains of H_x and vertices of D_x, and a many-to-one correspondence between directed edge of H_x and edges of D_x. Note that in the shrinking process we "preserve the embedding", i.e., the circular ordering of the edges around each vertex v of D_x is induced by the circular ordering of the directed edges "around" the maximal vertical chain of H_x corresponding to v. D_y is obtained analogously from H_y by shrinking the maximal horizontal chains (see Fig 6b).

Property 1. D_x and D_y are planar st-digraphs.

Theorem 8. *Let H be a turn-regular orthogonal representation of an embedded 4-planar graph, and let n be the number of vertices and bends of H. A planar orthogonal drawing of H with optimal area can be constructed in $O(n)$ time and space.*

Theorem 9. *Let H be a turn-regular orthogonal representation of an embedded 4-planar graph, and let n be the number of vertices and bends. A planar orthogonal drawing of H with optimal area $\mathcal{A}$ and whose total edge length is optimal among all drawings with area $\mathcal{A}$ can be constructed in $O(n^{7/4} \log n)$ time and $O(n)$ space.*

We recall that the minimum number of bends for an orthogonal representation of a 4-planar graph with n vertices is $O(n)$ [3, 29]. The algorithm described in [27] produces such an orthogonal representation, and there exist various algorithms for producing an orthogonal representation with a sub-optimal $O(n)$ number of bends (see, e.g, [4, 23, 28]).
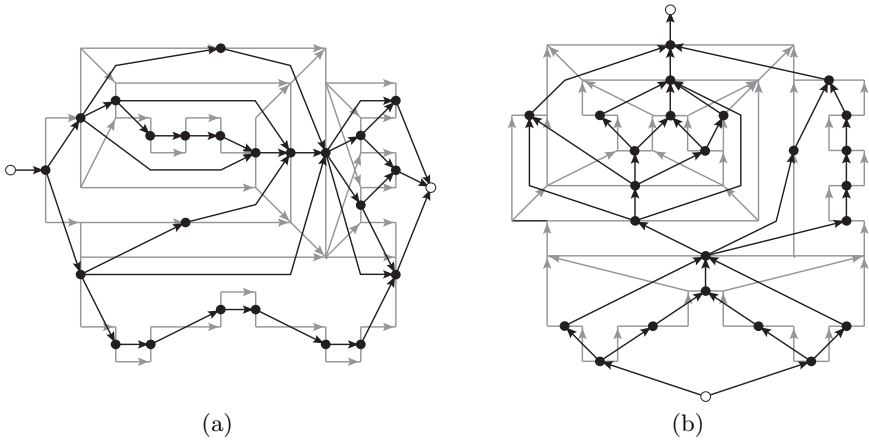
(a)   (b)

Fig. 6. (a) D_x. (b) D_y. The corresponding graphs H_x and H_y, from Fig. 5, are represented in grey.

7   Experiments

In this section, we present the results of an experimental study on a test suite of planar orthogonal representations of randomly generated biconnected 4-planar graphs. The analysis of the test suite has shown that the percentage of turn-regular faces is quite high. Motivated by this result, we have designed compaction heuristics based on the idea of "face turn-regularization".

7.1   Compaction Heuristics

We have implemented a compaction algorithm for orthogonal representations based on the results described in the previous sections. Namely, let H be a given orthogonal representation of an embedded 4-planar graph. The algorithm proceeds as follows:

- H is first tested for turn-regularity, using the algorithm described in Theorem 6.
- If H is turn-regular, the algorithm computes an orthogonal drawing of H with optimal area and optimal total edge length within that area by applying the techniques in Theorem 9.
- If H contains some faces that are not turn-regular, an algorithm is applied to make these faces turn-regular. The algorithm adds dummy vertices and edges to H, creating a new orthogonal representation H' that is turn-regular. The techniques in Theorem 9 are then used to find a drawing Γ' of H' with optimal area and optimal total edge length within that area. Finally, the dummy vertices and edges are removed from Γ' to yield an orthogonal drawing Γ of H. In general the orthogonal drawing Γ does not have optimal area and total edge length.

  Two simple approaches are used to make non-turn-regular faces turn-regular:

1. The first approach is an improvement of the standard rectangularization method described in [6, 27]. When a dummy edge is inserted, a dummy vertex is added only if it really needed. Each non-turn-regular face is divided into two or more smaller, rectangular faces.
2. The second approach recursively adds a straight edge (randomly chosen to be either horizontal or vertical) between each pair of kitty corners, until the face has been decomposed in smaller (but not necessarily rectangular) turn-regular faces. In general, this technique adds a much smaller number of dummy edges than the first approach.

In the following, we call the two heuristic compaction algorithms derived from the two turn-regularization approaches described above `Heur1` and `Heur2`, respectively. They are implemented in the *GDToolkit* library[4].

7.2 Test Suite and Experimental Results

Heuristics `Heur1` and `Heur2` were tested on a set of 530 randomly generated biconnected 4-planar graphs with number of vertices in the range $10\ldots3000$. The results are compared with a third compaction heuristic, `StdComp`, in which all faces, both turn-regular and not, are decomposed into rectangles using the rectangularization method of `Heur1`.

The graphs in the test suite have been generated with a technique used in other experimental studies on orthogonal drawings [1]. Each biconnected 4-planar graph is generated from a cycle of three vertices by performing a random series of *InsertVertex* and *InsertEdge* operations. The *InsertVertex* operation subdivides an existing edge into two new edges separated by a new vertex. The *InsertEdge* operation inserts a new edge between two existing vertices on the same face. Any biconnected planar graph can be generated by a sequence of these two operations. Also, for each graph to be generated, the density of the graph, i.e., the number of edges divided by the number of vertices, is randomly chosen before the generation algorithm is run.

Our first experiment consisted in studying the percentage of turn-regular faces in the graphs of our test suite. We have found that the percentage of turn-regular faces increases logarithmically with the density of the graphs, stabilizes at around 95%, and has an average value of 89% (see Fig. 7).

We have then analyzed the results of the three heuristics. In particular, we have considered, for `Heur1` and `Heur2`, the improvement in the drawing area, total edge length, and maximum edge length with respect to `StdComp`. `Heur2` performs better than `Heur1` in most cases; also, the improvement in area and total edge length of `Heur2` with respect to `StdComp` increases with the number of vertices of the graph (see Fig. 8). The average improvements of area and total edge length are 25% and 19%, respectively, for graphs with 3000 vertices; and there are some graphs in the test suite for which the area improvement is more than 45%.
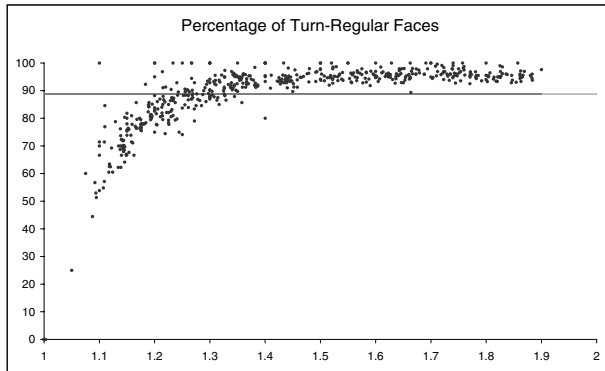
---

[4] http://www.dia.uniroma3.it/~gdt/

Fig. 7. The percentage of turn-regular faces of each graph. The x-axis indicates the density. The horizontal line indicates the average value.

We have also executed the three heuristics on a very large graph with $10,000$ vertices. The drawing computed by `Heur2` improves the area by 41% and the total edge length by 22% with respect to the drawing computed by `StdComp`.

8   Conclusions and Future Work

We introduced the notion of turn-regularity which allows the characterization of a class of orthogonal representations that are optimally compactable in terms of area in polynomial-time. In particular, given a turn-regular orthogonal representation of an embedded 4-planar graph, we provided a linear-time algorithm to compute a planar drawing with minimum area, and a polynomial-time algorithm to compute a planar drawing with optimal area and minimum total edge length within that area.

We provided several implementations of heuristics for making orthogonal representations turn-regular and we used them in the compaction algorithm, in place of the standard rectangularization step. Experiments on a randomly generated test suite of biconnected 4-planar graphs showed that the new compaction strategy performs much better than the standard one, especially for very large graphs.

The results presented in this paper motivate some future work, which includes:

- To continue the experimental study of the described heuristics on non-biconnected 4-planar graphs, comparing their behavior also with that of VLSI compaction algorithms.
- To investigate other effective heuristics for making an orthogonal representation turn-regular by adding a small number of edges.
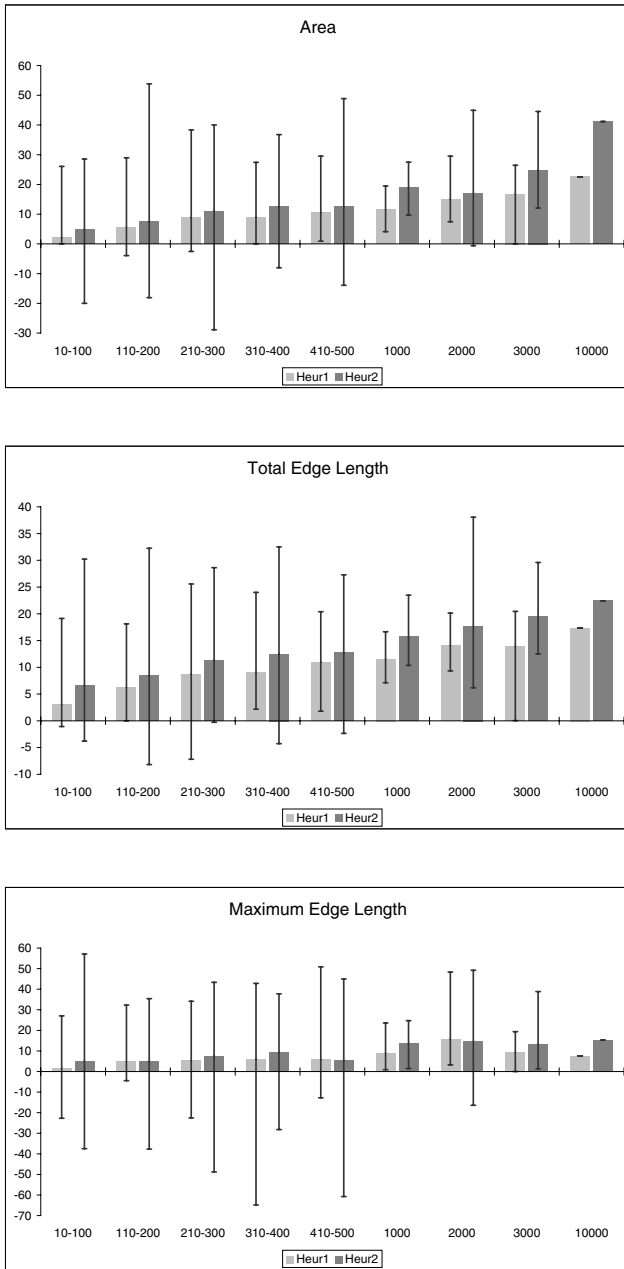
Fig. 8. The average percentage improvement in area, total edge length, and maximum edge length of `Heur1` and `Heur2` with respect to `StdComp`. The x-axes indicate the number of vertices. The interval lines indicate the minimum and maximum improvement.

– To find other families of orthogonal representations for which an optimal area drawing can be computed in polynomial time.
– The problem of computing an orthogonal representation with the minimum number of bends has been extensively investigated in a variable embedding setting [9, 11, 13]. It would be interesting to study the compaction problem when it is possible to change the embedding of the input graph.

Acknowledgments

References

[1] P. Bertolazzi, G. Di Battista, and W. Didimo. Computing orthogonal drawings with the minimum number of bends. In F. Dehne, A. Rau-Chaplin, J.-R. Sack, and R. Tamassia, editors, *Algorithms and Data Structures (Proc. WADS '97)*, volume 1272 of *Lecture Notes Comput. Sci.*, pages 331–344. Springer-Verlag, 1997.

[2] P. Bertolazzi, G. Di Battista, G. Liotta, and C. Mannino. Upward drawings of triconnected digraphs. *Algorithmica*, 6(12):476–497, 1994.

[3] T. C. Biedl. New lower bounds for orthogonal graph drawings. In F. J. Brandenburg, editor, *Graph Drawing (Proc. GD '95)*, volume 1027 of *Lecture Notes Comput. Sci.*, pages 28–39. Springer-Verlag, 1996.

[4] T. C. Biedl and G. Kant. A better heuristic for orthogonal graph drawings. *Comput. Geom. Theory Appl.*, 9(3):159–180, 1998.

[5] J. A. Bondy and U. S. R. Murty. *Graph Theory with Applications*. North-Holland, Amsterdam, The Netherlands, 1976.

[6] G. Di Battista, P. Eades, R. Tamassia, and I. G. Tollis. *Graph Drawing*. Prentice Hall, Upper Saddle River, NJ, 1999.

[7] G. Di Battista, A. Garg, G. Liotta, R. Tamassia, E. Tassinari, and F. Vargiu. An experimental comparison of four graph drawing algorithms. *Comput. Geom. Theory Appl.*, 7(5–6):303–325, 1997.

[8] G. Di Battista and G. Liotta. Upward planarity checking: "Faces are more than polygons". In S. H. Whitesides, editor, *Graph Drawing (Proc. GD '98)*, volume 1547 of *Lecture Notes Comput. Sci.*, pages 72–86. Springer-Verlag, 1998.

[9] G. Di Battista, G. Liotta, and F. Vargiu. Spirality and optimal orthogonal drawings. *SIAM J. Comput.*, 27(6):1764–1811, 1998.

[10] G. Di Battista and R. Tamassia. Algorithms for plane representations of acyclic digraphs. *Theoret. Comput. Sci.*, 61(2,3):175–198, 1988.

[11] W. Didimo and G. Liotta. Computing orthogonal drawings in a variable embedding setting. In K.-Y. Chwa and O. H. Ibarra, editors, *Algorithms and Computation (Proc. ISAAC '98)*, volume 1533 of *Lecture Notes Comput. Sci.*, pages 79–88. Springer-Verlag, 1998.

[12] U. Fößmeier and M. Kaufmann. Drawing high degree graphs with low bend numbers. In F. J. Brandenburg, editor, *Graph Drawing (Proc. GD '95)*, volume 1027 of *Lecture Notes Comput. Sci.*, pages 254–266. Springer-Verlag, 1996.

[13] A. Garg and R. Tamassia. Planar drawings and angular resolution: Algorithms and bounds. In J. van Leeuwen, editor, *Algorithms (Proc. ESA '94)*, volume 855 of *Lecture Notes Comput. Sci.*, pages 12–23. Springer-Verlag, 1994.

[14] A. Garg and R. Tamassia. On the computational complexity of upward and rectilinear planarity testing. In R. Tamassia and I. G. Tollis, editors, *Graph Drawing (Proc. GD '94)*, volume 894 of *Lecture Notes Comput. Sci.*, pages 286–297. Springer-Verlag, 1995.

[15] A. Garg and R. Tamassia. A new minimum cost flow algorithm with applications to graph drawing. In S. North, editor, *Graph Drawing (Proc. GD '96)*, volume 1190 of *Lecture Notes Comput. Sci.*, pages 201–216. Springer-Verlag, 1997.

[16] N. Gelfand and R. Tamassia. Algorithmic patterns for orthogonal graph drawing. In S. H. Whitesides, editor, *Graph Drawing (Proc. GD '98)*, volume 1547 of *Lecture Notes Comput. Sci.*, pages 138–152. Springer-Verlag, 1998.

[17] F. Harary. *Graph Theory*. Addison-Wesley, Reading, MA, 1969.

[18] F. Hoffmann and K. Kriegel. Embedding rectilinear graphs in linear time. *Inform. Process. Lett.*, 29(2):75–79, 1988.

[19] M. Y. Hsueh and D. O. Pederson. Computer-aided layout of lsi circuit building-blocks. In *Proc. IEEE Internat. Symp. Circuits and Systems*, 1979.

[20] G. W. Klau and P. Mutzel. Optimal compaction of orthogonal grid drawings. In G. Cornuejols, R. E. Burkard, and G. J. Woeginger, editors, *Integer Programming and Combinatorial Optimization (Proc. IPCO '99)*, volume 1610 of *Lecture Notes Comput. Sci.*, pages 304–319. Springer-Verlag, 1999.

[21] T. Lengauer. *Combinatorial Algorithms for Integrated Circuit Layout*. B. G. Teubner – John Wiley & Sons, Stuttgart, Germany – Chichester, England, 1990.

[22] R. H. J. M. Otten and J. G. van Wijk. Graph representations in interactive layout design. In *Proc. IEEE Internat. Sympos. Circuits and Systems*, pages 914–918, 1978.

[23] A. Papakostas and I. G. Tollis. Algorithms for area-efficient orthogonal drawings. *Comput. Geom. Theory Appl.*, 9(1–2):83–110, 1998. Special Issue on Geometric Representations of Graphs, G. Di Battista and R. Tamassia, editors.

[24] M. Patrignani. On the complexity of orthogonal compaction. In F. Dehne, A. Gupta, J.-R. Sack, and R. Tamassia, editors, *Algorithms and Data Structures (Proc. WADS '99)*, volume 1663 of *Lecture Notes Comput. Sci.*, pages 56–61. Springer-Verlag, 1999.

[25] J. M. Six, K. G. Kakoulis, and I. G. Tollis. Refinement of orthogonal graph drawings. In S. H. Whitesides, editor, *Graph Drawing (Proc. GD '98)*, volume 1547 of *Lecture Notes Comput. Sci.*, pages 302–315. Springer-Verlag, 1998.

[26] L. Stockmeyer. Optimal orientation of cells in slicing floorplan design. *Inform. Control*, 57(2/3):91–101, 1983.

[27] R. Tamassia. On embedding a graph in the grid with the minimum number of bends. *SIAM J. Comput.*, 16(3):421–444, 1987.

[28] R. Tamassia and I. G. Tollis. Planar grid embedding in linear time. *IEEE Trans. Circuits Syst.*, CAS-36(9):1230–1234, 1989.

[29] R. Tamassia, I. G. Tollis, and J. S. Vitter. Lower bounds for planar orthogonal drawings of graphs. *Inform. Process. Lett.*, 39(1):35–40, 1991.

[30] G. Vijayan and A. Wigderson. Rectilinear graphs and their embeddings. *SIAM J. Comput.*, 14(2):355–372, 1985.

[31] W. Wimer, I. Koren, and I. Cederbaum. Floorplans, planar graphs and layouts. *IEEE Trans. Circuits Syst.*, CAS-35(3):267–278, 1988.