Topic 14
Instruction-Level Parallelism and Processor Architecture

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This year, the Euro-Par conference is being held in beautiful Munich, Germany. I am very honored to welcome you to the instruction level parallelism and processor architecture sessions of Euro-Par 2000!

Instruction level parallelism (ILP) and processor architecture are important and growing fields. ILP research aims to extract very fine-grained parallelism not only from scientific code, but also from the irregular, general code that pervades applications and operating systems. Thus, successful ILP techniques can have a paramount effect on the performance of the entire computer system. ILP researchers in the academia and industry have continuously been designing leading-edge techniques to increase processor performance, such as microarchitecture enhancements, memory latency tolerance, and aggressive compiler algorithms. Samples of these techniques can be seen among the present collection of papers.

This year, 29 papers were submitted to the ILP and processor architecture topic. The selection process was very competitive, and difficult for the topic organizers. At the end, 4 submissions were accepted as regular papers, and 8 were accepted as short papers.

I would like to thank the other members of the organizing committee of the present topic, namely Prof. Theo Ungerer (the Local Chair), Prof. MariaGiovanna Sami, and Prof. Nader Bagherzadeh (the Vice-Chairs), who painstakingly reviewed many papers and provided insightful remarks. Prof. Ungerer took the lead in the publicity effort, set up an excellent Web-based review database for the papers, and at the end represented us during the Euro-Par program committee meeting. I am also grateful to our referees for lending us their expertise and providing rigorous reviews. I would finally like to thank the Euro-Par 2000 conference organizers for their continued support.

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