Research Article

Investigating PDP-based error by testing NAND and D-Latch based on CNTFET (Stanford model)

Salimeh Shahrabadi[1]

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Abstract
This paper uses Stanford model for MOS-like CNTFET in order to find optimum values of its parameters. The purpose is to test well-designed NAND and D-Latch ICs based on this optimized CNTFET at $V_{DD} = 0.9$ V in 32-nm technology by HSPICE, in order to observed PDP-based error (power–delay product-based error). This error causes a growth in power consumption of logic gates and circuits. Importance of using "trade-off factor" instead of "PDP factor" in some specific cases is clearly illustrated in this paper. The optimum values of MOS-like CNTFET parameters which are obtained in by Stanford model this paper, are the same as the optimum ones in previous works. This research displays a useful insight about MOS-like CNTFET and PDP-based error and presents trade-off factor to making well-designed gates and circuits.

Keywords MOS-like CNTFET · Stanford model · HSPICE · NAND · D-Latch · PDP · Trade-Off · Nanoscience · Nanotechnology

1 Introduction

The first integrated circuit (IC) based on transistors was built in 1958. Over time, the dimensions of these transistors have become smaller and their structures have changed. FINFET, nanowire FET, carbon nanotube FET (CNTFET), etc., are some examples of these new structures. In fact, the ultimate goal is to manufacture an improved IC with smallest dimensions, less power consumption, lower cost, simplest structure, and highest processing speed. Some researchers have endeavored to investigate on different models of both CMOS and CNTFET, design some logic gates by using them, and compare their results. For example, they compared:

- CMOS and standard-CNTFET [1]
- CMOS and CNTFET [2–6]
- C-CMOS (Conventional CMOS), FINFET, and MOS-like CNTFET [7]
- C-CMOS and CNTFET [8]
- CMOS and MOS-like CNTFET [9]

By testing the logic gates and circuits (such as AND, OR, MUX, full adder) which were based on CMOS and CNTFET [1–9], researchers declared that CNTFET models can provide better results than CMOS models because they can reduce average power, delay, PDP (power–delay product), increase performance speed, and occupy less volume in ICs. These studies were done in different conditions:

- In 0.18 µm,32 nm and 16 nm process technologies [1, 5–7]
- At different power supply voltages ($V_{DD} = 0.5$ V, 0.65 V, 0.7 V, 0.8 V or 0.9 V) [4, 5, 7, 8]
- Changing the gate-source voltage ($0 \leq V_{GS} \leq 0.6$ V) [4]
- Testing by HSPICE or Cadence software [1, 3, 5, 7, 9]

Given the advantages of CNTFET over CMOS (according to [1–9]), MOS-like CNTFET (Stanford model [7, 9]) is selected and investigated in this paper. For beginning,

✉ Salimeh Shahrabadi, salimehshahrabadi@yahoo.com | [1]Department of Electrical and Electronic Engineering, Islamic Azad University, Science and Research Branch, Tehran, Iran.

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I study its parameters in NAND structure by HSPICE at $V_{DD} = 0.9$ V and $f_{data} = 250$ MHz, in 32 nm technology. This paper does not present new model for CNTFET or compare MOS-like CNTFET with other kinds, but it tries to find optimum values for CNTFET parameters by the Stanford model code, illustrate the error of PDP factor and also present "trade-off factor" instead of "PDP factor" in some specific cases. These optimum values for each parameter (pitch, N, and chiral vector) leads to have improved MOS-like CNTFET and optimized NAND gate. Then, a D-Latch (data latch or D-type latch) based on this NAND is tested in order to design an optimized IC with low average power and delay. During this process, the error is displayed. This process shows that this CNTFET (due to its optimized parameters) will provide high performance even in a complicated IC such as FPGA, to make it optimum.

2 Optimum design and test results

2.1 MOS-like CNTFET (Stanford model: HSPICE)

When channel length of MOSFET reaches bellow 10 nm, we actually will face a limit [10]. CNTFET is one of the choices because of its semiconducting and current-carrying properties [10]. Well-controlled channel, high ON current, easily design, and implementation of multi-threshold structures with less complexity are the main advantages of CNTFET over MOSFET [7]. MOS-like CNTFET, which is shown in Fig. 1, has a similar structure as MOSFET. Parameters L_{ch}, W_{gate}, L_{dd}, L_{ss}, Pitch, and N are, respectively, channel length, channel width, nanotubes length between gate and drain, nanotubes length between gate and source, distance between two adjoining nanotubes, and the number of nanotubes (see Fig. 1a). Parameters N and pitch define I_{CNT} (the current from drain to source) and W_{gate}. These two parameters actually determine the CNTFET dimensions, speed and power consumption, so their values should be selected according to delay and average power. Another important factor in CNTFETs is diameter of nanotubes (D_{CNT}) that has effect on I_{CNT}(on). This factor is usually presented by chiral vector. The related equations are [7, 11]:

$$W_{gate} = \mathrm{Max}\left(W_{min}, N \times \mathrm{Pitch}\right) \tag{1}$$

$$D_{CNT} = \frac{\sqrt{3}}{\pi} a_0 \sqrt{m^2 + n^2 + mn} \tag{2}$$

$$\text{Chiral Vector} = (m, n) \tag{3}$$

$$\text{Threshold Voltage} = V_{th} = \frac{0.43}{D_{CNT}} \tag{4}$$

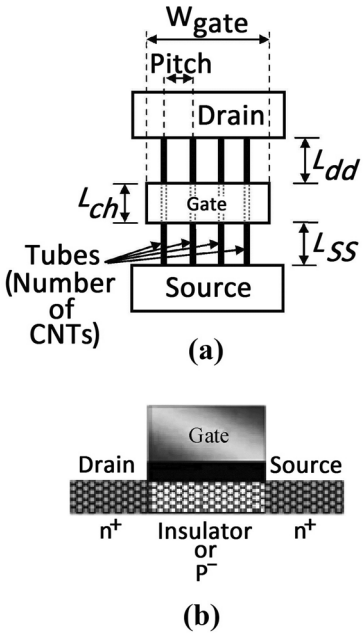
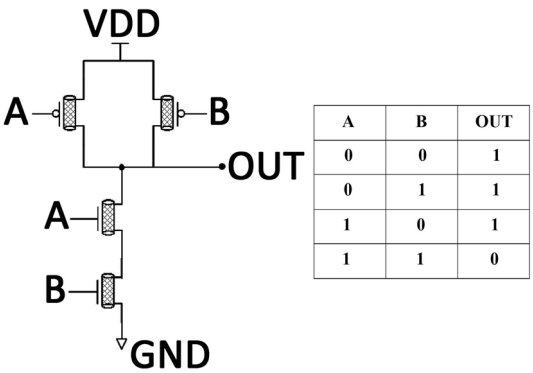


Fig. 1 **a** The CNTFET schematic, **b** the structure of a MOS-like CNTFET [7]



A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 2 The structure of a two-input NAND based on CNTFET [7]

$$I_{CNT} = \frac{N \times g_{CNT} \times \left(V_{DD} - V_{th}\right)}{1 + \left(g_{CNT} \times L_s \times \rho_s\right)} \tag{5}$$

The coefficient a_0 is distance between two carbon atoms (≈ 0.142 nm), and the parameters m and n are integers which show the chirality of nanotube. Value of V_{th} changes with CNTFET diameter so each CNTFET can have its own V_{th} in an IC. The parameters g_{CNT},L_s and ρ_s are, respectively, transconductance, source length, and source–carrier density (Fig. 2). Investigation on MOS-like CNTFET-based ICs is done by Stanford model (in 32-nm technology) because it includes practical non-idealities such as scattering,

inter-CNT charge screening effects, the channel length dependence of current drive, the geometry dependence of the gate-to-channel capacitance, the interconnect wiring capacitance, the source/drain series resistance and their contact resistance, and also parasitic effects, apart from accurate predictions of dynamic and transient performance with more than 90% accuracy [12–14]. The simulations are carried in HSPICE software at $V_{DD} = 0.9$ V and $f_{data} = 250$ MHz and results are explained in subsections 2.2 and 2.3. The error based on PDP (power–delay product) factor is illustrated too.

2.2 NAND gate

In this study, I design a NAND gate based on four MOS-like CNTFETs and set its pitch at 5 nm. After testing its delay, average power, and PDP at different values of N, the process is repeated for pitch = 10 nm and pitch = 20 nm to observe effects of the N-changes and pitch changes on the NAND properties. The test results are placed in Table 1, and their curves are shown in Fig. 3. The increase in N causes the delay reduction and average power growth, because the number of current path is added. Thus there are two options to have an optimized NAND:

- According to PDP factor, the optimum value for N is 9 because we have the minimum PDP at this number (see Table 1).
- According to the delay and average power factors, the optimum value for N is 3 because there is a best trade-off between delay and power consumption (see Fig. 3 and Table 1).

At $N = 9$, the power consumption is approximately doubled, but the delay just has 1-ps improvement than $N = 3$, and therefore, the number 9 is not optimum value of N. PDP is not really a good factor for investigating properties of one kind of transistor (such as MOS-like CNTFET) or one kind of logic gate (such as NAND). But when the comparison is between two or more kinds of transistors or between two or more kinds of logic gates, using PDP factor can speed up the comparison process without occurring any error. For instance, the comparison between "C-CMOS-based NAND" and "TG-based NAND" which is done by PDP results [7]. Even for testing logic circuits (e.g., D-Latch, full adder, shift register, SRAM, FPGA, etc.) which are composed of different gates, PDP factor is also useful [5]. As a result, in this condition, $N = 3$ is the optimum value, and the trade-off between delay and average power is the best factor. Now the effects of pitch and chiral vector changes at $N = 3$ should be checked.

Based on Table 1 results, the growth in the pitch value reduces the delay and increases the power consumption, but because of current saturation, this procedure is not intense and the values are close together. This phenomenon is observed again when the effect of pitch changes is studied at chiral vector (19, 0) and $N = 3$ that its results are placed in Table 2. We have the best trade-off between delay and average power at pitch = 10 nm. Notice that in this case, PDP factor has the same result as trade-off factor, and both of them show that 10 nm is the optimum value of pitch, but it does not mean that the PDP can be a proper factor for testing one kind of transistor or logic gate. By reduction of the pitch value, the coating effect between nanotubes increases, and it causes an enhancement in the capacitance of parasitic capacitors between nanotubes, and therefore, we observe the delay increase and current decrease (power reduction) in Table 2.

The final step for designing an improved NAND based on optimized MOS-like CNTFET is to peruse the effects of chiral vector changes at $N = 3$ and pitch = 10 nm. As stated in Sect. 2.1 (Eq. 2, 3), the chiral vector represents the diameter of nanotubes, for example, (19, 0) is equal to 1.478 nm [7]. According to Table 3, the increase in nanotubes diameter causes the current enhancement, so it raises the power consumption. The PDP factor chooses

Table 1 The effects of N changes on the CNTFET-based NAND properties at chiral vector (19, 0)

N	at Pitch = 5 nm			at Pitch = 10 nm			at Pitch = 20 nm		
	Delay (10^{-12} S)	Average power (10^{-8} W)	PDP (10^{-19} j)	Delay (10^{-12} S)	Average power (10^{-8} W)	PDP (10^{-19} j)	Delay (10^{-12} S)	Average power (10^{-8} W)	PDP (10^{-19} j)
1	6.461	3.007	1.943	6.006	3.004	1.804	5.878	2.986	1.755
3	**2.572**	**3.709**	0.9538	**2.3**	**3.8**	0.87	**2.235**	**3.971**	0.8874
6	1.584	4.399	0.697	1.371	5.052	0.6927	1.327	5.516	0.732
9	1.217	5.225	**0.6356**	1.062	6.141	**0.6519**	1.023	6.751	**0.69**
12	1.029	6.289	0.647	0.9022	7.426	0.67	0.8768	7.881	0.691
15	0.9143	7.12	0.6509	0.8016	8.622	0.6912	0.7803	9.167	0.7153
18	0.8317	8.123	0.6756	0.738	9.864	0.728	0.7156	10.33	0.7392

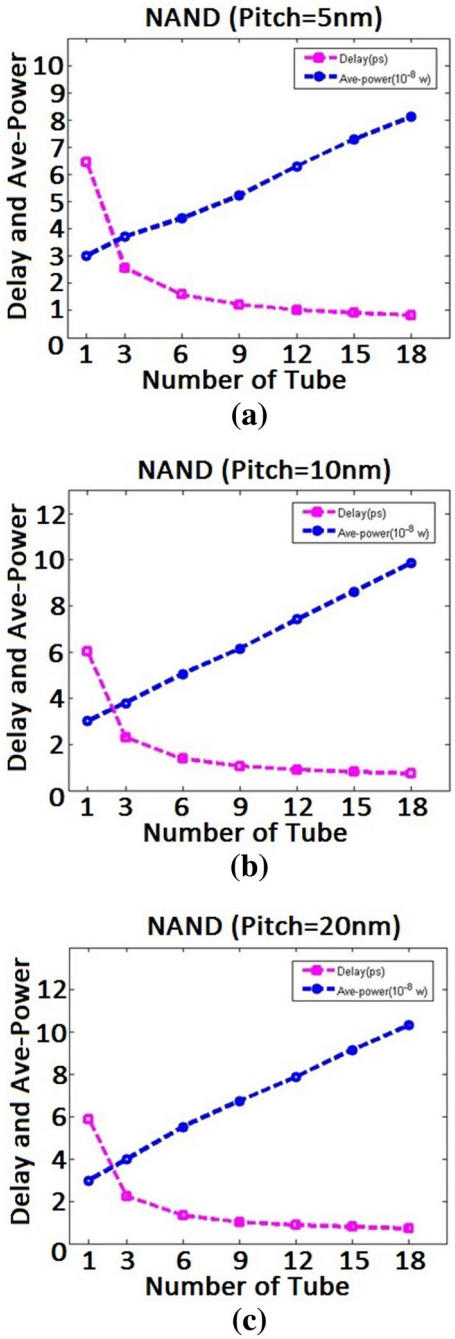


Fig. 3 The delay and average power curves of the MOS-like CNTFET-based NAND at: **a** Pitch = 5 nm, **b** Pitch = 10 nm, **c** Pitch = 20 nm

the vector (25, 0) as the optimum chiral vector. But Figs. 4, 5 (based on Table 3) show that the vector (19, 0) has the best trade-off between delay and average power. If we select the vector (25, 0), the power consumption increases in exchange for 0.5 ps less delay, than the vector (19, 0). Thus the error of using PDP factor shows itself again. As a result, the optimum values for MOS-like CNTFET are $N = 3$, pitch = 10 nm and the chiral vector (19, 0) which lead to have an improved NAND. These results are achieved in previous works that proves their validity, such as [7] and [11] which, respectively, proposes the chiral vectors "(19, 0) and (22, 0)" and "(10, 0), (19, 0) and (29, 0)" for CNTFET but "trade-off factor" in this paper shows why (19, 0) is better. In fact, I use CNTFET (Because of its advantages over MOSFET) and Stanford model (for its non-idealities) to make a well-designed NAND and display the error of using "PDP factor". NANDs are universal gates that it means all other gates and circuits, e.g.,

Table 2 The effects of pitch changes on the CNTFET-based NAND properties at chiral vector (19, 0) and $N = 3$

Pitch (nm)	Delay (10^{-12} S)	Ave. power (10^{-8} W)	PDP (10^{-19} j)
5	2.5	3.7	0.925
10	**2.3**	**3.8**	**0.874**
15	2.28	3.9	0.889
20	2.23	3.95	0.880

Table 3 The effects of chiral vector changes on the CNTFET-based NAND properties at pitch = 10 nm and $N = 3$

Chiral vector (m, n)	Delay (10^{-12} S)	Ave. power (10^{-8} W)	PDP (10^{-19} j)
(8, 0)	24	3.35	8
(10, 0)	8.75	3.43	3
(13, 0)	4.6	3.71	1.7
(15, 0)	3.7	3.88	1.4
(19, 0)	**2.3**	**3.8**	0.87
(22, 0)	2.1	4	0.84
(25, 0)	1.8	4.5	**0.81**
(32, 0)	1.71	5.19	0.89

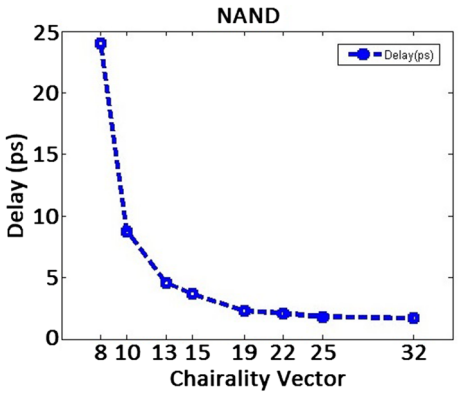


Fig. 4 The Delay curve of the MOS-like CNTFET-based NAND at $N = 3$ and Pitch = 10 nm

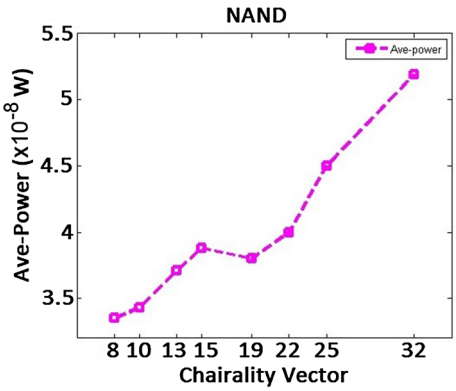


Fig. 5 The Ave.power curve of the MOS-like CNTFET-based NAND at $N = 3$ and Pitch = 10 nm

memories and FPGAs, can be designed optimally by this gate if we make it optimum!

HSPICE simulation for this optimized NAND is done by CNTFET library (in 32 nm technology based on Stanford model) at $V_{DD} = 0.9^{V}$ and $f_{data} = 250^{MHz}$ which its waveforms are displayed in Fig. 6. The results match table in Fig. 2. It is important to note that, based on Eq. 5, we can have better power consumption at lower V_{DD} because I_{CNT} will decrease. In subsection 2.3, an improved D-Latch based on this optimized NAND is tested.

2.3 D-Latch IC

D-Latch (data latch) is the smallest element of memory which can store one bit (0 or 1) in itself and its performance

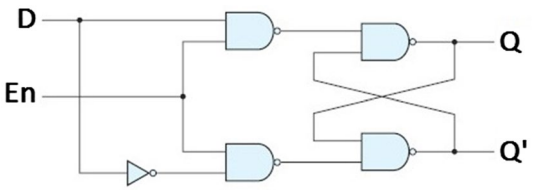


Fig. 7 The structure of a D-Latch based on NAND

is near to D-FF (delay flip-flop). As pictured in Fig. 7, it consists of four optimized NAND and one optimized NOT (which can be made by 1 optimized NAND). Clock pulse and data are applied to the "*En*" and "*D*" input ports, respectively. Data storage occurs at $EN = 0$ and its release on Q output port occurs at $EN = 1$. Output of the port Q'

Table 4 The effects of N changes on the CNTFET-based D-Latch properties at pitch = 10 nm and the chiral vector (19, 0)

N	Delay (10^{-12} S)	Ave. power (10^{-7} W)	PDP (10^{-19}j)
1	5.673	0.4805	0.27
3	**5.348**	**0.4759**	**0.25**
6	5.227	4.651	4.2
9	5.191	6.667	3.46
12	5.173	8.605	4.45
15	5.162	10.64	5.49
18	5.156	12.68	6.53
22	5.151	14.79	7.61

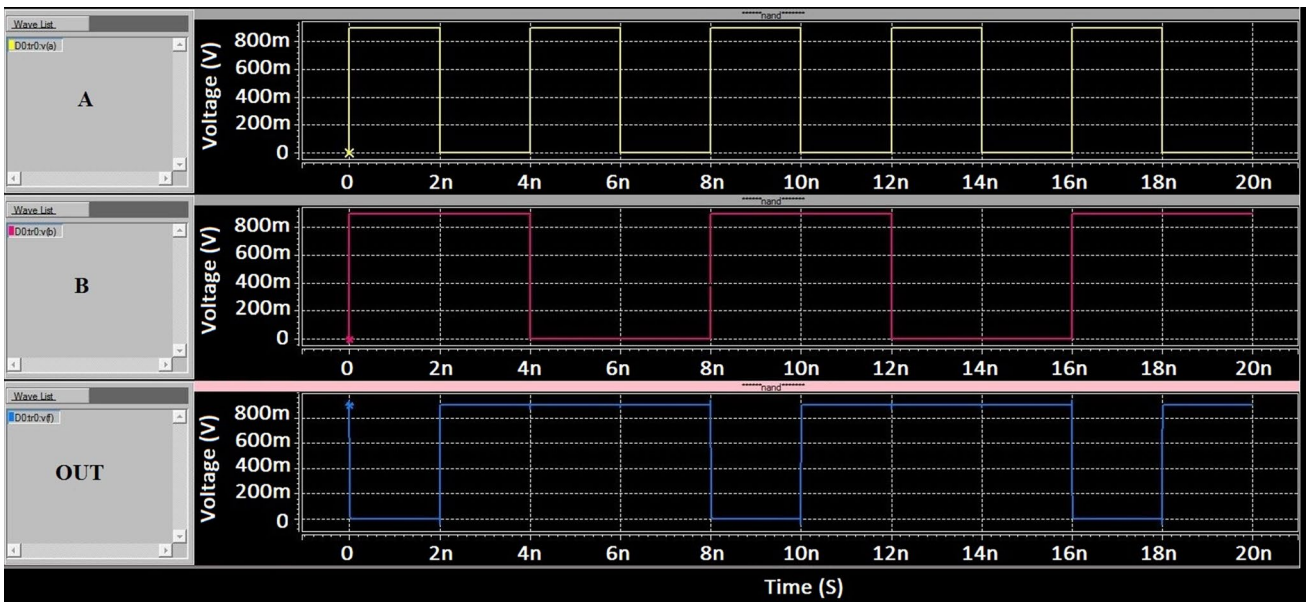


Fig. 6 The input and output waveforms of this improved NAND (by HSPICE simulator), $f_{data} = 250$ MHz

Table 5 The effects of pitch changes on the CNTFET-based D-Latch properties at $N=3$ and the chiral vector (19, 0)

Pitch (nm)	Delay (10^{-12} S)	Ave. power (10^{-7} W)	PDP (10^{-19} j)
5	5.37	1.36	0.73
10	**5.34**	**0.4759**	**0.25**
15	5.41	3.462	1.87
20	5.46	2.398	1.309

Table 6 The effects of chiral vector changes on the CNTFET-based D-Latch properties at Pitch = 10 nm and $N=3$

Chiral vector (m, n)	Delay (10^{-12} S)	Ave. power (10^{-7} W)	PDP (10^{-19} j)
(8, 0)	30.58	0.757	2.3
(10, 0)	14.03	0.895	1.25
(13, 0)	8.962	1.261	1.13
(15, 0)	7.966	1.721	1.37
(19, 0)	**5.348**	**0.475**	**0.25**
(22, 0)	4.779	2.924	1.39
(32, 0)	4.552	2.939	1.33

is the reverse of *Q*. Effects of N, pitch, and chiral vector changes are observable in Tables 4, 5, 6 respectively. All three tables show that "trade-off" and "PDP" factors have the same result. Both of them refer to $N=3$, pitch = 10 nm, and chiral vector (19, 0). This fact proves that PDP is a useful factor to test the performance of a logic circuit (like D-Latch), not a logic gate or a transistor.

Assume we choose $N=9$ instead of $N=3$ (see Table 1), so the power consumption becomes approximately doubled in one NAND. Then for a D-Latch with four NAND and one NOT, the power consumption becomes at least 10 times higher. Table 4 displays that the average power at $N=9$ is equal to 6.667×10^{-7} W which is 14 times higher than the average power at $N=3$. Figure 8 shows input and output waveforms of this improved D-Latch that its HSPICE Simulation is done by CNTFET library (in 32-nm technology based on Stanford model) at $V_{DD} = 0.9^{V}$, $f_{CLK} = 1^{GHz}$ and $f_{data} = 250^{MHz}$. This research demonstrates that this optimized MOS-like CNTFET will provide low power consumption and high processing speed even in complicated circuits such as memories, FPGAs, and processors.

3 Conclusion

After discovering the new carbon structure (C60) in 1985 and making the carbon nanotubes (CNTs) in 1991, the first CNT-based transistor was built in 1998. Its new models have been designed by the efforts of researchers that MOS-like CNTFET is one of these models. This paper tests NAND and D-Latch based on MOS-like CNTFET by HSPICE based on Stanford model in 32-nm technology, and tries to find optimum values of this CNTFET parameters in order to have an optimized universal gate (NAND) which can

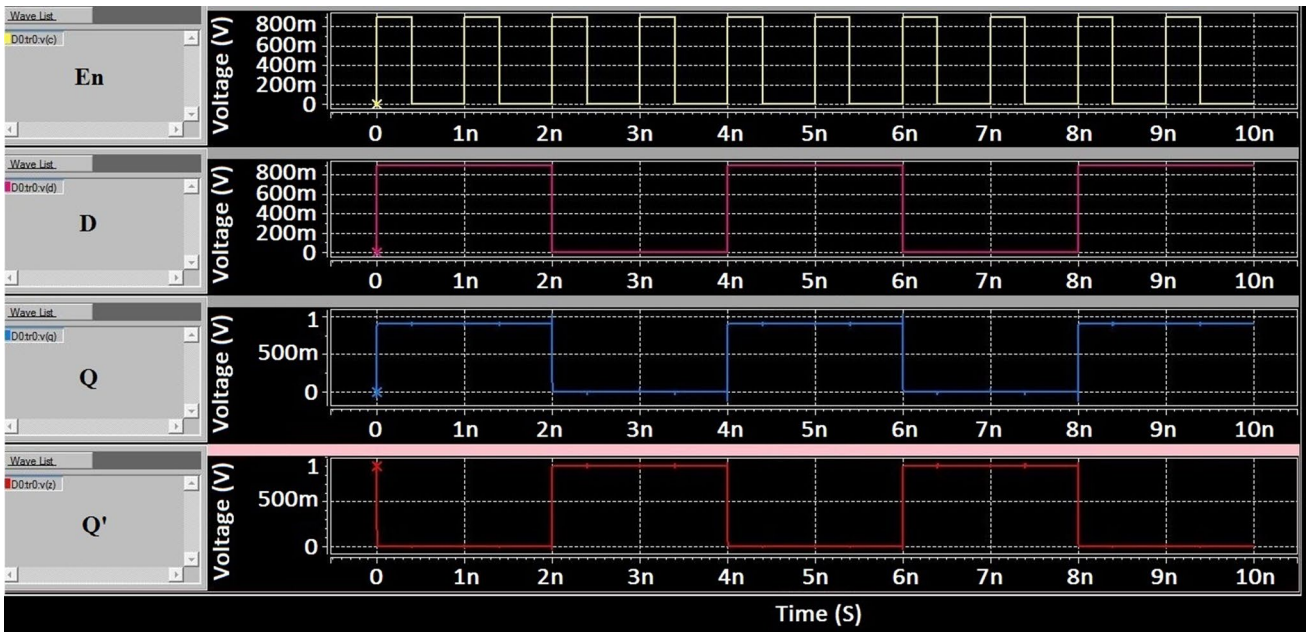


Fig. 8 The input and output waveforms of this improved D-Latch (by HSPICE simulator), $f_{CLK} = 1$ GHz, $f_{data} = 250$ MHz

provide an optimized ICs such as D-Latch, D-FF, memory, FPGA. It also shows that the usage of PDP factor for considering one transistor (such as MOS-like CNTFET) or one logic gate (such as NAND) causes an important error which can intensely enhance power consumption at complicated ICs. This study does not present new model for CNTFET, but it tries to design improved gates and ICs according to PDP and trade-off factors and explains why, for example, the chiral vector (19, 0) is proper than (10, 0), (22, 0) and (29, 0) because all of them were proposed related works. As a result, it presents the trade-off between delay and average power as a proper factor to make them optimized. But also it emphasizes that for investigation one logic circuits (such as D-Latch), or for comparison between two or more kinds of transistors or two or more kinds of logic gates, using PDP factor can speed up our test process without occurring any error. The optimum values for a MOS-like CNTFET (based on the Stanford model) are $N = 3$, pitch = 10 nm and the chiral vector (19, 0).

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Compliance with ethical standards

Conflict of interest The author declares that there is no conflict of interest associated in this manuscript.

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