Application of thyristor controlled phase shifting transformer excitation impedance switching control to suppress short-circuit fault current level

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Abstract Short-circuit fault current suppression is a very important issue in modern large-interconnected power networks. Conventional short-circuit current limiters, such as superconducting fault current limiters, have to increase additional equipment investments. Fast power electronics controlled flexible AC transmission system (FACTS) devices have opened a new way for suppressing the fault current levels, while maintaining their normal functionalities for steady-state and transient power system operation and control. Thyristor controlled phase shifting transformer (TCPST) is a beneficial FACTS device in modern power systems, which is capable of regulating regional power

flow. The mathematical model for TCPST under different operation modes is firstly investigated in this study. Intuitively, the phase shifting angle control can adjust the equivalent impedance of TCPST, but the effect has been demonstrated to be weak. Therefore, a novel transformer excitation impedance switching (EIS) control method, is proposed for fault current suppressing, according to the impedance characteristics of TCPST. Simulation results on IEEE 14-bus system have shown considerable current limiting characteristic of the EIS control under various fault types. Also, analysis of the timing requirement during fault interruption, overvoltage phenomenon, and ancillary mechanical support issues during EIS control is discussed, so as to implement the proposed EIS control properly for fast fault current suppression.

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1 Introduction

Power system short-circuit fault current level has kept rising due to a variety of reasons, such as the increasing demand for electricity with economic development [1, 2], increasing installed generation capacity of power systems, increasing construction of the transmission network, etc. The peak value of short-circuit fault current is the primary concern for selecting power circuit breakers and other power equipments [3, 4]. When the short-circuit current level reaches some certain extent, there will be no optional equipment due to the limitations of existing power equipment manufacturing technology or considerations on

equipment cost. Therefore, short-circuit fault current magnitude expansion has become a nonnegligible problem of large interconnected power systems. To suppress the fault current level has become one of the research hotspots in modern power system operation and control area.

There are two possible stages to handle the short-circuit current increasing issue, one is power system level, through network operation and reconfiguration; and the other is component level, through the application of additional fault current limiting power equipments.

For the first power system operation and reconfiguration related method, power engineers may adopt the following techniques, such as: using higher voltage level, which might reduce the fault current level with equal MVA capacity; performing load shedding and islanding operations when permitted [5], which can separate the system into some smaller subsystems with lower short-circuit level; or applying intelligent switchgear for smart transmission switching under the smart grid environment [4, 6], etc.

In practice, it is always not so easy to suppress the short-circuit fault current by power system level operation and control in real-time, because the slower speed of system level scheduling. However, the response of fault current limiting devices is always much faster, and various models of fault current limiters have been designed during the last few decades, including:

- 1) Superconducting fault current limiters (SFCL), when the fault current value exceeds the conductor's critical value, they can change their resistance values from the superconducting state to the resistive state very fast [7, 8].
- 2) Microprocessor-controlled fault current limiters [9–12], which might be comprised of either LC resonant circuits or reactors, and they can also adjust their impedances during faults.
- 3) Current limiting type fuses, they can be considered as nonlinear resistances that are able to force a current zero rapidly [13–15].
- 4) The current limiters based on FACTS type devices, for example, thyristor controlled series compensation (TCSC), which is able to limit the current by increasing the series inductance of the attached lines [16]. Interphase power controller (IPC) that is composed of a conventional phase-shifting transformer (PST) and a static synchronous series compensator, and it has the ability of short-circuit current mitigation and power flow control [17]. Bridge-type fault current limiter (BFCL) that uses a switched transformer-type DC reactor, whilst the load current exceeds a predefined threshold, the secondary side of the transformer can be opened by an insulated gate bipolar transistor [18].

These FACTS type devices have possible capability of being applied for fault current suppression, because they can perform power flow regulation functions under steady-state operation conditions [19], and can also be switched to an emergency control status during serious faults. Thyristor-controlled phase shifting transformer (TCPST) is a special FACTS device with a series and a parallel power transformer, which fulfills fast phase angle adjustment of the voltage across the device to regulate regional power flow [20–22]. However, the fault current suppressing capability for the TCPST device has seldom been referred by past researches. Since the investments on TCPST would be rather expensive, it is necessary to perform other functions besides voltage phase shifting and power flow controlling, such as short-circuit current suppressing, considering the fast control properties of power electronic switches inside the TCPST.

The structure of this paper is as follows. The varying equivalent impedance of TCPST is derived in Section 2, according to the working mode of the power electronic switches. The phase shifting angle (PSA) control for fault current limiting, is briefly analyzed in Section 3. Since it has been proven to have not very good suppression effect on the short-circuit fault current in our previous work [20], a novel short-circuit fault current suppression method named as transformer excitation impedance switching (EIS) control is proposed, based on the varying impedance characteristics of TCPST. Simulation results have shown that the novel EIS control method has a more remarkable current suppressing performance. Then, Section 4 evaluates the potential interruption time sequence for power circuit breakers and the mechanical support issues that might be induced by the EIS control scheme. Finally, the conclusions are given in Section 5.

2 Modeling of TCPST based on its equivalent impedance

Power system PSTs usually comprise of two transformers to fulfill voltage phase angle shifting operation, one parallel excitation transformer (ET) and one series booting transformer (BT). The two transformers can be connected through wye-wye or wye-delta wiring, then the voltage vector of the BT winding is able to be regulated by the switching control circuit, which can turn the original voltage vector into a different voltage vector with the objective amplitude and phase angle. Two types of common connections for PSTs are shown in Fig. 1. Typically, if the input (i) and output (j) of the PST have equal voltage amplitudes, it is called a symmetric type PST, as shown in Fig. 1b. Otherwise, it is asymmetric type PST, as shown in Fig. 1a.

Fig. 1 Two types of different wiring topologies for PSTs

The control circuit of PSTs might have plenty of different topology structures, with different operation mechanisms and mathematical models correspondingly; several types of controllable PSTs can be obtained in the relevant literatures [23–25]. Due to space limit, it is not suitable to analyze every different types of PSTs in-depth about their influence on short-circuit fault current suppression, or their effectiveness as new types of short-circuit current limiters. Therefore, one newer type of PST, named two core symmetrical discrete phase shifting transformer (TCSD type PST) [25], is chosen in this study to investigate its potential for short-circuit fault current suppression.

The main electrical circuit of TCPST (short for TCSD type PST in this study) is presented in Fig. 2a, which contains a transformer (ET) in parallel, a transformer (BT) in series, and the power electronics control circuit to switch among different connection modes [26, 27]. To make it more convenient for writing, the ET winding connected directly to the transmission line is named primary winding E1, and the winding that has magnetic coupling with the primary winding E1 is called secondary winding, which can be divided into three parts, denoted by E2, E3 and E4. The taps ratio of ET's secondary winding E2 and E3 and E4 is set as 1:3:9. BT's primary winding is separated into two segments, named as B1 and B2 respectively; the secondary winding for BT is expressed as B3. The connection topology of the power electronic switches for ET's three secondary windings is shown in Fig. 2b. Different on/off status combinations of the electronic switches can provide

Fig. 2 Main circuit for TCSD type thyristor-controlled PST

27 operation modes T , corresponding to 27 different phase shifting angle values ϕ . To fulfill the function of voltage regulation, the tap positions of ET's secondary winding can be adjusted through the 12 power electronic switches inside the switching control circuit. Each power electronic switch contains a pair of reverse parallel thyristors, the structural diagram is shown in Fig. 2c. The detailed relationship between operation mode T and the status of the three ET's secondary windings are listed in Fig. A1 and Table A1 in "Appendix A". It should be noted that the power thyristors used in this study are taken as ideal switches, neglecting the transients and harmonics inside these power electronic devices.

In this TCSD type thyristor-controlled PST, the “T” shape equivalent circuit is developed to unify the voltage reference point for transformers BT and ET, and the equivalent circuit considering all windings’ impedances is shown in Fig. 3. Assuming that the three-phase parameters for the TCPST are symmetric, make Z_{B1} , Z_{B2} , Z_{B3} , Z_{E1} and Z_T be BT and ET’s winding impedances of the TCPST, and Z_{BM1} , Z_{BM2} and Z_{EM} denote respectively the excitation impedances for transformers BT and ET.

According to Fig. 3, the turns ratio of the BT winding can be expressed as:

$$\begin{cases} \frac{U_{B3}}{U_{B1}} = \frac{N_{B3}}{N_{B1}} = n_B \\ \frac{U_{B3}}{U_{B2}} = \frac{N_{B3}}{N_{B2}} = n_B \end{cases} \quad (1)$$

where U_{B1} , U_{B2} , U_{B3} are the induced voltage amplitudes for BT’s windings 1, 2, 3, respectively; N_{B1} , N_{B2} , N_{B3} are the numbers of turns of the BT’s windings, respectively; n_B is the turn ratio for BT winding 3 to 1, or 3 to 2. These number of turns are determined by transformer design, and the turns ratio is decided by the system phase-shifting angle taps, all the number of turns and turns ratio values are fixed constants after the completion of phase shifter manufacturing.

The turns ratio of transformer ET is:

$$\frac{U_{E1}}{U_T} = \frac{N_{E1}}{TN_T} = n_T \quad T = \pm 1, \pm 2, \dots, \pm 13 \quad (2)$$

where U_{E1} is the voltage magnitude of ET’s primary winding; U_T is the voltage magnitude of ET’s secondary winding; n_T is the corresponding turns ratio under

operation mode T ; N_{E1} is the number of turns for the transformer ET’s primary winding; N_T is the number of turns inside each tap of the transformer ET’s secondary winding.

For BT’s primary side, the original winding is separated into two equal segments, it is obvious to acquire the following magnetic potential balance equation, while ignoring the exciting current.

$$N_{B1}\dot{I}_{B1} + N_{B2}\dot{I}_{B2} + N_{B3}\dot{I}_{B3} = 0 \quad (3)$$

According to (1), we have:

$$\dot{I}_{B1} + \dot{I}_{B2} + n_B\dot{I}_{B3} = 0 \quad (4)$$

where $\dot{I}_{B1}$ and $\dot{I}_{B2}$ are the currents through windings B1 and B2; $\dot{I}_{B3}$ is the current of BT’s secondary winding.

Under operation mode T , the current magnitude of ET’s primary and secondary winding has the following relationship:

$$\frac{I_T}{I_{E1}} = \frac{N_{E1}}{TN_T} = n_T \quad (5)$$

Considering the symmetric characteristic of three phase currents, it can be derived that:

$$\dot{I}_{E1a} = -\frac{\dot{I}_{Ta}}{n_T} = -\frac{1}{n_T}(\dot{I}_{B3b} - \dot{I}_{B3c}) = j\frac{\sqrt{3}}{n_T}\dot{I}_{B3a} \quad (6)$$

Thus, the current of ET’s primary winding $\dot{I}_{E1}$ in the single-phase expression is:

$$\dot{I}_{E1} = j\frac{\sqrt{3}}{n_T}\dot{I}_{B3} \quad (7)$$

At the point “O” of Fig. 3, the current relationship can be written as:

$$\dot{I}_{E1} = \dot{I}_{B1} - \dot{I}_{B2} \quad (8)$$

Eliminating the current of BT’s secondary winding $\dot{I}_{B3}$, and considering (3), (7) and (8), we have:

$$\dot{I}_{B2} = \frac{1 + j\sqrt{3}/(n_T n_B)}{1 - j\sqrt{3}/(n_T n_B)} \dot{I}_{B1} \quad (9)$$

$$\dot{I}_{E1} = \frac{2\sqrt{3}}{\sqrt{3} + jn_T n_B} \dot{I}_{B1} \quad (10)$$

From (9), the currents through windings B1 and B2, namely $\dot{I}_{B1}$ and $\dot{I}_{B2}$ are equal, so the phase shifting angle φ can be defined as:

$$e^{j\varphi} = \frac{1 + j\sqrt{3}/(n_T n_B)}{1 - j\sqrt{3}/(n_T n_B)} \quad (11)$$

Considering the turns ratios in (1) and (2), the angle φ can be further expressed as:

Fig. 3 “T” shape equivalent circuit of transformers BT and ET considering impedances of all windings

$$\varphi = 2 \arctan \frac{\sqrt{3}}{n_T n_B} = 2 \arctan \left(\frac{\sqrt{3} N_{B2} N_T}{N_{B3} N_{E1}} T \right) \quad (12)$$

Therefore, (9) can be rewritten as a function of the phase shifting angle φ :

$$\dot{I}_{B2} = e^{j\varphi} \dot{I}_{B1} \quad (13)$$

According to Ohm's Law, the voltage relationship across the TCPST can be obtained from Fig. 3. The voltage vector of the supplying end (SA, letter A denotes for phase a) can be expressed by the voltage vector of the loading end (LA) and the impedances in between:

$$\dot{U}_S = (\dot{U}_{B1} + \dot{I}_{B1} Z_{B1}) + (\dot{U}_{B2} + \dot{I}_{B2} Z_{B2}) + \dot{U}_L \quad (14)$$

Since the BT's primary winding is equally separated as two parts on the iron core, the induced electromotive force on the two segments are equal, namely that $\dot{U}_{B1} = \dot{U}_{B2}$, $Z_{B1} = Z_{B2}$, thus (14) can be rewritten as:

$$\dot{U}_L = \dot{U}_S - 2\dot{U}_{B1} - \dot{I}_{B1} Z_{B1} (1 + e^{j\varphi}) \quad (15)$$

Eliminating the induced voltage amplitudes of $\dot{U}_{B1}$ for BT's winding 1 in (15), the port voltage on phase a of BT's secondary winding yields:

$$\begin{aligned} \dot{U}_{B3a} + \dot{I}_{B3a} Z_{B3} &= (\dot{U}_{Tb} + \dot{I}_{Tb} Z_T) - (\dot{U}_{Tc} + \dot{I}_{Tc} Z_T) \\ &= -j\sqrt{3}(\dot{U}_{Ta} + \dot{I}_{Ta} Z_T) \\ &= -j\sqrt{3} \left(\frac{\dot{U}_{E1a}}{n_T} - n_T \dot{I}_{E1a} Z_T \right) \end{aligned} \quad (16)$$

Taking into consideration the ratio between BT and ET transformers in (7), it is able to eliminate the variable $\dot{I}_{B3a}$ in (16):

$$\dot{U}_{E1a} = (n_T^2 Z_T + \frac{1}{3} n_T^2 Z_{B3}) \dot{I}_{E1a} + j \frac{n_T}{\sqrt{3}} \dot{U}_{B3a} \quad (17)$$

Similar derivation can be done phases b and c, therefore, the voltage relationship can be expressed in single-phase description:

$$\dot{U}_{E1} = (n_T^2 Z_T + \frac{1}{3} n_T^2 Z_{B3}) \dot{I}_{E1} + j \frac{n_T}{\sqrt{3}} \dot{U}_{B3} \quad (18)$$

Based on the circuit diagram in Fig. 3, we have:

$$\dot{U}_O = \dot{U}_{E1} + \dot{I}_{E1} Z_{E1} \quad (19)$$

From (18) and (19), it is easy to get:

$$\dot{U}_O = (Z_{E1} + n_T^2 Z_T + \frac{1}{3} n_T^2 Z_{B3}) \dot{I}_{E1} + j \frac{n_T}{\sqrt{3}} \dot{U}_{B3} \quad (20)$$

Also, from the current relationship in (10), it can be obtained that:

$$\begin{aligned} \dot{U}_O &= (Z_{E1} + n_T^2 Z_T + \frac{1}{3} n_T^2 Z_{B3}) \frac{2\sqrt{3}}{\sqrt{3} + j n_T n_B} \dot{I}_{B1} \\ &\quad + j \frac{n_T n_B}{\sqrt{3}} \dot{U}_{B1} \end{aligned} \quad (21)$$

Eliminating the variable of $\dot{U}_O$ by (22):

$$\dot{U}_S - \dot{U}_O = \dot{U}_{B1} + \dot{I}_{B1} Z_{B1} \quad (22)$$

Then $\dot{U}_{B1}$ can be expressed as a function of variables $\dot{U}_S$ and $\dot{I}_{B1}$:

$$\begin{aligned} \dot{U}_{B1} &= \frac{\sqrt{3}}{\sqrt{3} + j n_T n_B} \dot{U}_S - \frac{\sqrt{3}}{\sqrt{3} + j n_T n_B} \\ &\quad \times \left[(Z_{E1} + n_T^2 Z_T + \frac{1}{3} n_T^2 Z_{B3}) \frac{2\sqrt{3}}{\sqrt{3} + j n_T n_B} + Z_{B1} \right] \dot{I}_{B1} \end{aligned} \quad (23)$$

Substituting (23) into (15), it can be reformulated as:

$$\begin{aligned} \dot{U}_L &= \frac{-\sqrt{3} + j n_T n_B}{\sqrt{3} + j n_T n_B} \dot{U}_S - \{ (1 + e^{j\varphi}) Z_{B1} \\ &\quad - \frac{2\sqrt{3}}{\sqrt{3} + j n_T n_B} \left[(Z_{E1} + n_T^2 Z_T + \frac{1}{3} n_T^2 Z_{B3}) \frac{2\sqrt{3}}{\sqrt{3} + j n_T n_B} + Z_{B1} \right] \} \dot{I}_{B1} \\ &= \frac{-\sqrt{3} + j n_T n_B}{\sqrt{3} + j n_T n_B} \dot{U}_S - \left\{ \frac{-\sqrt{3} + j n_T n_B}{\sqrt{3} + j n_T n_B} Z_{B1} + e^{j\varphi} Z_{B1} \right. \\ &\quad \left. + \frac{-\sqrt{3} + j n_T n_B}{\sqrt{3} + j n_T n_B} \left[\frac{12}{(n_T n_B)^2 + 3} (Z_{E1} + n_T^2 Z_T + \frac{1}{3} n_T^2 Z_{B3}) \right] \right\} \dot{I}_S \end{aligned} \quad (24)$$

Noting that the expression of (11), then the mathematical model of this type of TCPST can be expressed as an ideal phase shifter in series with an equivalent impedance:

$$\begin{aligned} \dot{U}_L &= \dot{U}_S e^{j\varphi} - \dot{I}_S e^{j\varphi} \\ &\quad \times \left[2Z_{B1} + \frac{12}{(n_T n_B)^2 + 3} (Z_{E1} + n_T^2 Z_T + \frac{1}{3} n_T^2 Z_{B3}) \right] \\ &= \dot{U}_S e^{j\varphi} - \dot{I}_L Z_{eq} \\ &= (\dot{U}_S - \dot{I}_S Z_{eq}) e^{j\varphi} \end{aligned} \quad (25)$$

$$\begin{cases} Z_{eq} = 2Z_{B1} + \frac{12}{(n_T n_B)^2 + 3} \left(Z_{E1} + n_T^2 Z_T + \frac{1}{3} n_T^2 Z_{B3} \right) \\ \varphi = 2 \arctan \frac{U_{B1}}{U_{E1}} = 2 \arctan \frac{\sqrt{3}}{n_T n_B} = 2 \arctan \left(\frac{\sqrt{3} N_{B2} N_T}{N_{B3} N_{E1}} T \right) \end{cases} \quad (26)$$

where the equivalent series impedance Z_{eq} and phase shifting angle φ can be expressed by all the original parameters in Fig. 3; Z_{E1} , Z_{B1} , Z_{B3} , Z_T are the impedances of the corresponding windings; the parameters in small

letters of n_T , n_B are the corresponding turns ratio defined in (1) and (2); the parameters in capital letters of N_{E1} , N_{B2} , N_{B3} , N_T are the number of turns in the corresponding windings.

Equation (26) shows the mathematical model of this type of TCPST considering all the winding impedances, and the simplified equivalent circuit are plotted in Fig. 4.

When the influence of the windings' resistances are neglected, and assuming that the winding leakage reactance for each tap of ET secondary winding is X_0 , the equivalent impedances can then be rewritten as:

$$\begin{cases} Z_{eq} = jx_{eq} \\ Z_T = jT^2 X_0 \\ n_T = N_{E1}/(TN_T) \end{cases} \quad (27)$$

The simplified equivalent reactance of TCPST can be formulated in a relationship with the operation mode T :

$$x_{eq}(T) = X_F - \frac{X_V}{K_1 + K_2 T^2} \quad (28)$$

The computational coefficients of X_F , X_V , K_1 and K_2 in (28) can be obtained as:

$$\begin{cases} X_F = 2X_{B1} + 4 \left[X_{E1} + \left(\frac{N_{E1}}{N_T} \right)^2 X_0 \right] = 2X_{B1} + 4X_{E1} + 4 \left(\frac{N_{E1}}{N_T} \right)^2 X_0 \\ X_V = 4(N_{E1}n_B)^2 X_{E1} + 4 \left(\frac{N_{E1}}{N_T} \right)^2 (N_{E1}n_B)^2 X_0 - 4N_{E1}^2 X_{B3} \\ K_1 = (N_{E1}n_B)^2 \\ K_2 = 3N_T^2 \end{cases} \quad (29)$$

Considering the zero operation mode $T = 0$, therefore, the equivalent reactance can be further expressed in a whole as:

$$x_{eq}(T) = \begin{cases} X_F - \frac{X_V}{K_1 + K_2 T^2} & T = \pm 1, \pm 2, \dots, \pm 13 \\ 2X_{B1} + \frac{4X_{B3}}{n_B^2} & T = 0 \end{cases} \quad (30)$$

From (25) to (30), it can be drawn that:

- 1) The equivalent series impedance of the TCPST varies with the phase shifting angle φ , which is also related

Fig. 4 Simplified equivalent circuit diagram for TCPST according to mathematical model

to the operation mode T of the power electronic switches on the ET's secondary side.

- 2) Since the orthogonal connection of transformers BT and ET only has the electromagnetic coupling effect, the impedance expression of Z_{eq} in (26) does not have practical physical meaning, it is only an equivalent mathematical formulation.
- 3) The equivalent impedance Z_{eq} for operation mode 0 can also be calculated through (26), by assuming transformer ET's tap ratio n_T to infinity.
- 4) By applying the equivalent impedance Z_{eq} of TCPST, the terminal voltage vector across the supplying and loading ends, is related to both the phase shifting angle φ , and the line transmitted currents. However, most researches have neglected the varying impedance of TCPST during steady-state and transient studies in the past [23–26].

3 Effect of EIS control on short-circuit current suppression

According to the mathematical modeling of TCPST in Section 2, a very natural way to suppress the fault current levels on the transmission lines by TCPST, is the phase shifting angle (PSA) control method. The current suppression effect by PSA control can be referred to our previous paper [20]. However, the current limiting capability of PSA control seems not high enough to assist the fault interrupting for power circuit breakers. Therefore, another method by transformer EIS control is presented in this study.

3.1 Principle of transformer EIS control

According to (30), the equivalent series impedance Z_{eq} of the TCPST varies with the operation mode T of the control circuit. The novel EIS control principle is to adjust the control circuit to the operation mode $T = 0$. It can be drawn from Fig. 2 and Fig. 3 that, when stopping the triggering pulse for the parallel transformer ET's secondary winding, namely, blocking all power electronic devices, the parallel transformer ET's secondary side will enter the open-circuit status. Under this mode $T = 0$, the transformer ET's tap ratio n_T can be seen as infinity, thus the equivalent circuit can be simplified to Fig. 5, according to positive sequence fault analysis. And it can be clearly seen that the EIS control means to insert a huge impedance into the transmission line between supplying end S and loading end L.

As the series transformer BT's secondary winding is connected to parallel transformer ET's secondary side in

Fig. 5 Simplified equivalent circuit under open-circuit condition of BT's secondary winding

Fig. 6 Equivalent impedance under open-circuit condition of BT's secondary winding

this situation, thus the delta connection for the series transformer BT's secondary winding is suspended, looking like that it is also open-circuit, then the equivalent circuit can be further simplified to Fig. 6.

It can be observed from Fig. 6 that, when BT's secondary winding is open-circuit, the equivalent impedance of the TCPST becomes:

$$Z_{\text{TCPST}} = Z_{B1} + Z_{BM} + Z_{B2} \quad (31)$$

where $Z_{BM} = Z_{BM1} + Z_{BM2}$ is the combination of BT's excitation impedances, in series with its leakage impedance Z_{B1} and Z_{B2} , together forms the equivalent impedance under the open-circuit condition of BT's secondary winding.

Because of the extremely large value of excitation impedance Z_{BM} for typical transformers, the proposed EIS control can be used to limit the short-circuit current to a rather small value. Noting that $i_{B1}^{(1)} = i_{B2}^{(1)}$ in this situation, none phase shifting angle is applied during EIS control, only the huge impedance in (31) is applied in the

transmission line, which is a completely new control scheme for short-circuit fault current suppression.

3.2 TCPST parameter description

According to the mathematical model and equivalent circuit of TCPST in the previous section, the simulation parameters are chosen according to a base voltage of 525 kV and base capacity of 100 MVA. The three phase capacity for the TCPST is 2274 MVA, with a symmetric type, the switching modes as ± 13 , and the rated shifting angle is $\pm 25^\circ$. All the other parameters for this TCSD type PST are acquired from Electric Power Research Institute of Shanghai Electric Power Company [28], as listed in Table 1.

3.3 Validation of EIS control under various fault types

PSCAD simulation is used to test the short-circuit current suppression effect by the proposed EIS control method. The test system is IEEE 14-bus standard system, and only one TCPST is applied to the line 13–14. Impose a three-phase symmetrical short-circuit fault at 0.2 s on transmission line 13–14 close to the bus 14 side. Assuming the identification of short-circuit fault is exactly at 0.2 s instantaneously, and the switching time of ET's secondary side power electronic devices is set as 0.01 s after the fault. The simulated three phase transient current waveforms are shown in Fig. 7a, with the red, blue and green curves denote the corresponding three phases, respectively. It can be seen in Fig. 7a that, the amplitudes of the short-circuit current are greatly reduced after the application of EIS control of TCPST, the peak current value of the first cycle is about 19.33 kA (without EIS control of TCPST), and it can be reduced to about 4.56 kA in the following cycles (with EIS control of TCPST), which means that the current amplitude has decrease by about 76.4%, the results are also given in Table 2.

Table 1 Simulation parameters of TCPST

Parameters	Series transformer BT	Parallel transformer ET
Rated capacity (MVA)	3×378	3×439
Rated voltage grid side (kV)	$130.78/\sqrt{3}$	$525/\sqrt{3}$
Rated voltage thyristor side (kV)	231.25	$20.71/\sqrt{3}$ for winding E2, $62.13/\sqrt{3}$ for winding E3, $186.39/\sqrt{3}$ for winding E4
Rated current grid side (kA)	2.5	1.448
Rated current thyristor side (kA)	1.633	2.828
Percentage of impedance voltage (%)	11	14
Connection type	Δ/Δ	YN/Y

Fig. 7 Short-circuit current simulation by EIS control with BT's secondary side open

Table 2 Short-circuit current suppression effect of EIS control of TCPST

Short-circuit current peak values	Three-phase fault	Two-phase fault	Double phase-grounded fault	Single phase-grounded fault
Without EIS control (kA)	19.33	14.94	— 19.55	19.33
With EIS control (kA)	4.56	3.72	— 7.03	7.35
Decrease percentage (%)	76.4	75.1	64.0	62.0

Similarly, applying different types of faults, respectively the two-phase short-circuit, double phase-grounded short-circuit, and single phase-grounded short-circuit, to the same faulted location as in Fig. 7a, the simulated short-circuit current waveforms are shown from Fig. 7b, 7c, 7d. It can be seen from the three sub-figures that, the amplitudes of the short-circuit current peak values are greatly reduced, from about 14.94 kA, — 19.55 kA and 19.33 kA (without EIS control of TCPST), to about 3.72 kA, — 7.03 kA and 7.35 kA (with EIS control of TCPST), for these three faulted scenarios. And the short-circuit current amplitude will decrease by 75.1%, 64.0% and 62.0%, respectively.

3.4 Comparison of EIS control with PSA control methods

It can be seen from Fig. 7 that, before excitation impedance being injected to the system, the instantaneous value of short-circuit current goes extremely high as the peak value is several times bigger of its rated peak value before 0.2 s. After 0.21 s, the secondary side of the series transformer BT is switched to an open-circuit condition, fault current decreases enormously due to the influence of transformer excitation impedance, to about 1/4 of its original short-circuit current peak value. It can be seen in Table 2 that the fault current suppression can reach of 62.0% to 76.4%, much more effective than the effect of below 10% of PSA control in our previous researches [20]. Because the series transformer's secondary side is switched to an open-circuit status by EIS control, the TCPST can act as a new type of short-circuit current limiter.

4 Discussion

Through EIS control, TCPST can be acted as a new type of short-circuit current suppresser for power system secure operation, it might also have several potential issues from the viewpoint of power equipments, including fault interruption time requirements for power breakers and the potential ancillary mechanical support.

4.1 Time sequence analysis for fault clearing

The prerequisite of using EIS control of TCPST to suppress short-circuit fault current level is that, it has to complete the operation mode adjustment before the interrupting operation of high voltage circuit breakers; otherwise, it would be of no use to the power breakers. The time sequence for protective relay operation and breaker interruption has been shown in Fig. 8. In the first period, the action of protective relays including short-circuit fault

Fig. 8 Interruption sequence for high voltage circuit breakers

identification, calculation time of protection setting, tripping delay; and then an opening instruction is given to circuit breakers according to safety setting parameters of the protective relays. During the interruption period of circuit breakers, the short-circuit opening time includes two parts: the contact parting time, and the arcing time before current zero, according to standard ANSI/IEEE-C37.010.

According to another standard IEC-62271, breaker inherent breaking time is usually provided by the manufacturer. As for the 500 kV level breakers, i.e. Siemens Germany 3AP live tank circuit breaker is not more than two fundamental cycles 40 ms [29], Pinggao Electric China LW6-550 series breaker has an inherent breaking time of 28 ms [30]. And the triggering pulse for modern power electronic devices can be as fast as less than 10 ms [31, 32], which is sufficient to implement the proposed transformer EIS control method before the contact separation of breakers so as to interrupt a comparatively small short-circuit fault current.

4.2 Overvoltage analysis for proposed EIS control

PSCAD simulations are performed to investigate the overvoltage phenomenon induced by the EIS control operation of TCPST. Since the EIS control is initiated by blocking all power electronic devices on the parallel transformer ET's secondary side, the protection of the switching circuit is not part of this study. Then the overvoltage analysis is performed to check the tolerability of both of the TCPST transformers during the proposed EIS control.

The TCPST current and voltage parameters are the same with Section 3.3, take the most serious three phase fault as an example, the phase voltage curves of ET's and BT's secondary side during fault are shown in Fig. 9.

As shown in Fig. 9a, the fault also occurs at 0.2 s as the previous simulations, the peak voltage of the ET secondary side under normal operation is very close to 0 kV, because the equivalent series impedance Z_{eq} is rather small so as to transmit power through TCPST to the loading end. Then EIS control initiated at 0.21 s, the ET's secondary side

Fig. 9 Phase voltages of ET's and BT's secondary side before and after EIS control

works as open-circuit, the voltage peak value of phase a reaches up to $170.4/\sqrt{2} = 120.5$ kV, which does not exceed the system voltage level $525/3 = 175$ kV. However, in Fig. 9b, the voltage peak value of phase a of BT's secondary side ramps up to about $309.2/\sqrt{2} = 218.6$ kV after EIS control, 1.637 times larger than the rated designing value of $231.25/\sqrt{3} = 133.51$ kV, which might impose great challenge to the insulation and protection of BT transformer.

Typically, surge arresters and multi-column MOVs in parallel, are suggested to avoid overvoltage phenomenon for FACTS devices, during actual power system transient operations [33]. However, since the BT transformer are not selected equal to the 500 kV system voltage level, the overvoltage and insulation issue would be no big problem for our TCPST, as analyzed below:

- 1) After applying EIS strategy, it can be seen in Fig. 9 that the high-frequency switching overvoltage (SOV) is not apparent on both ET and BT's secondary side because the EIS control is only stopping the firing of the electronic switches. The transformer is able to withstand several times of switching overvoltage as it is usually no bigger than the lightning impulse. The basic insulation level (BIL) are typically 3 to 5 times of the system voltage for lightning impulse on power equipments according to IEEE Std C62.82.1 [34]. And for the short duration temporary overvoltage (TOV) induced by the open-circuit control, the

transformers of 121 kV level is able to withstand 230 kV of the temporary overvoltage, and the value can reach up to 275 kV for the 145 kV level by IEEE Std C62.82.1 [34]. Therefore, it is feasible to select the 230 kV-withstanding type transformer for the BT in our TCPST (275 kV-withstanding type would be more qualified for this study), which is larger than the 218.6 kV overvoltage during the EIS control.

- 2) As for the power electronic devices inside the TCPST, generally each power electronic switch contains a RC-snubber circuit for overvoltage protection. On the other hand, because the breakthrough voltage of thyristor is very close to its rated voltage, the rated voltage of the thyristor should always retain a certain margin through the planning stage, typically 2 to 3 times of the withstand peak voltage [35]. The overvoltage under EIS control in this study is no bigger than 2 times of the phase-ground voltage of the TCPST in our simulations. Therefore, the SOV and TOV overvoltage will not exert damage on the thyristors.

4.3 Other potential issues for proposed EIS control

It is also worth noting that, the proposed EIS control scheme cannot avoid the first-cycle peak of the fault current as typical fast current-limiting fuses do, because of the approximate 10 ms time required for operation mode switching of the power electronic devices. Thereby, it might not reduce the electrodynamic forces induced by the peak current of the first cycle, and possible mechanical support are still needed for the transformer design for the TCPST.

In addition, the switching transient duty for thyristors in the TCPST is beyond the scope of this study, and many previous prototype tests have been performed for power electronic switches in other FACTS devices, such as TCSC [16], IPC [17], etc., to provide fast and reliable switching during short-circuit transients of power systems. The main contribution of this study is providing new thoughts of changing the equivalent series impedance of TCPST that is associated with the transmission line, thus suppressing the short-circuit fault current level when the power breakers are ordered to interrupt the fault.

5 Conclusion

In order to suppress the power system short-circuit fault current level, a novel fault current suppression control scheme for TCPST is proposed, without installing any additional power equipments. From the electric circuit of one typical TCPST, the varying equivalent impedance

properties are analysed theoretically, according to different operation modes of the power electronic switches. The transformer EIS control is then proposed, by opening the secondary winding of transformer ET after the fault being detected, the TCPST can act as a large impedance being injected to the associated transmission line. Through mathematical analysis and simulation, fault current suppression by the EIS control has shown more excellent current limiting capability by reducing the fault current by 62.0% to 76.4% within one cycle, comparing with those of no more than 10% by PSA control of TCPST [20]. Further analysis for the fault clearing time sequence and possible mechanical support issues, is also discussed so as to implement the proposed EIS control appropriately for fast fault current suppression.

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Appendix A

The bidirectional power electronic switches connected to E2, E3 and E4 can make different combinations of winding topologies with different impedances; the switches in red are “on”, and switches with “off” state are not plotted.

See Fig. A1 and Table A1.

Fig. A1 Two typical operation modes with their corresponding on/off status of twelve bidirectional power electronic switches

Table A1 Different voltage output of parallel transformer ET secondary side with different operation modes of E2, E3, E4

T	E2	E3	E4	Taps	T	E2	E3	E4	Taps
0	×	×	×	0 + 0 + 0 = 0					
1	+	×	×	1 + 0 + 0 = 1	- 1	-	×	×	1 + 0 + 0 = - 1
2	-	+	×	- 1 + 3 + 0 = 2	- 2	+	-	×	1 - 3 + 0 = - 2
3	×	+	×	0 + 3 + 0 = 3	- 3	×	+	×	0 - 3 + 0 = - 3
4	+	+	×	1 + 3 + 0 = 4	- 4	-	-	×	- 1 - 3 + 0 = - 4
5	-	-	+	- 1 - 3 + 9 = 5	- 5	+	+	+	1 + 3 - 9 = - 5
6	×	-	+	0 - 3 + 9 = 6	- 6	×	+	-	0 + 3 - 9 = - 6
7	+	-	+	1 - 3 + 9 = 7	- 7	-	+	-	- 1 + 3 - 9 = - 7
8	-	×	+	-1 + 0 + 9 = 8	- 8	+	×	-	1 + 0 - 9 = - 8
9	×	×	+	0 + 0 + 9 = 9	- 9	×	×	-	0 + 0 - 9 = - 9
10	+	×	+	1 - 3 + 9 = 10	- 10	-	×	-	1 + 3 - 9 = - 10
11	-	+	+	-1 + 3 + 9 = 11	- 11	+	-	-	1 - 3 - 9 = - 11
12	×	+	+	0 + 3 + 9 = 12	- 12	×	-	-	0 - 3 - 9 = - 12
13	+	+	+	1 + 3 + 9 = 13	- 13	-	-	-	- 1 - 3 - 9 = - 13

Note: “ × ” means off state; “+” and “-” denote that the ET’s secondary winding has the same or different end with the primary winding. Then taps of the transformer ET’s secondary winding can be achieved by combination of E2, E3 and E4, corresponding to 27 operation modes

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