Elastically Stretchable Insulation and Bilevel Metallization and Its Application in a Stretchable *RLC* Circuit

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Stretchable electronics need stretchable wiring membranes that are equivalent to printed wiring boards but with elastically stretchable insulators and multilevel metallization. We have developed technology for elastically stretchable two-level metallization on an elastomeric membrane. Two levels of conductors were separated by a photopatternable elastomeric dielectric and connected through via holes. They were evaluated at uniaxial tensile strains of up to 30% and then used to create an elastomeric resistor–inductor–capacitor (*RLC*) circuit, whose alternating-current (AC) response was measured at biaxial tensile strains of up to 6%. We describe the fabrication process, morphology, and electrical performance of the bilevel metallization and the *RLC* circuit.

Key words: Thin film, stretchable conductors, bilevel conductors, resonant circuit

INTRODUCTION

Stretchable Electronics Need Elastically Stretchable Insulation and Multilevel Metallization

Stretchable conductors are key components in numerous emerging technologies, including biomedical applications,^{1–3} stretchable interconnects,^{4,5} and electronic skin.⁶ Stretchable conductors add qualitatively new capabilities to electronic circuitry that are not possible with rigid electronics⁷ because of their inherent flexibility, durability, biocompatibility, and conformability.

Gold films on the silicone elastomer, poly(dimethylsiloxane) (PDMS), are often used as stretchable conductors in these applications. Three fundamentally distinct types of stretchable gold conductors have been developed on PDMS: (1) meander-shaped gold conductors (15 μm thick) akin to a two-dimensional spring,⁸ (2) wavy gold conductors that are deposited on prestretched

PDMS,^{9,10} and (3) straight microcracked gold conductors (20 nm to 100 nm thick).¹¹ Microcracked gold conductors have several advantages, a major one being that microcracked films can be stretched isotropically, whereas both meander-shaped and wavy gold conductors can only be stretched anisotropically. Also, the deposition and patterning of microcracked gold films can be accomplished with standard microfabrication technology without requiring mechanical prestrain⁹ or electrodeposition of a thick gold film. Lithographic patterning of a nearly flat microcracked film is more accurate than that of a buckled film. Furthermore, microcracked films show low fatigue and isotropically stretch and relax for at least 250,000 cycles.¹²

The maximum strain at which a microcracked film remains electrically conducting decreases with decreasing width and length of the conductor. On relaxed PDMS, the microcracks in the gold film are 0.5 μm to 2 μm long. When strained, the microcracks coalesce. The electrical current is interrupted if the coalescing microcracks span the width of the conductor. The probability of this occurring increases with decreasing width and length of the

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Table I. Physical properties at room temperature of Au,¹⁶ polydimethyl siloxane (PDMS),¹⁷ and photopatternable silicone (PPS),¹⁸ the materials used as the metallization, substrate, and interlevel dielectric of our bilevel metallization

Property	Bulk Au	PDMS	PPS
Young's modulus	78 GPa	2 MPa	160 MPa
Electrical conductivity	4.52×10^7 S/m	3.4×10^{-13} S/m	Very low
Dielectric constant	N/A	2.65	3.2

conductor. In particular, gold conductors that are $<20 \mu\text{m}$ wide typically do not remain conducting beyond 5% to 10% strain, thus limiting wiring density. Therefore, to achieve high wiring density, multilevel metallization akin to printed circuit boards is required.

By efficient wire routing, multilevel metallization enables a high density of components on a circuit board. This is why conventional electronics rely on printed wiring boards with multiple metal layers that are separated by rigid insulators. Analogously, stretchable electronics need stretchable wiring membranes with insulators and elastically stretchable multilevel metallization. Here we present the building blocks for elastically stretchable multilevel metallization in the form of stretchable bilevel metallization for an elastomeric wiring membrane. The two levels are connected through via holes in the elastomeric interlevel dielectric. We demonstrate the functionality of our bilevel metallization technology with a stretchable resistor–inductor–capacitor (*RLC*) circuit.

This paper describes two consecutive projects. The first project demonstrates the fabrication of an elastomeric bilevel metallization test structure and its evaluation under strain. The second project applies this new technology to the fabrication of an elastomeric *RLC* circuit. The electrical properties of the circuit and its components are measured at various strains and compared with calculated values based on a proposed equivalent circuit. We begin by describing the geometry of the bilevel metallization, its fabrication, evaluation, and results. Then we describe the geometry of the *RLC* circuit, its fabrication, expected properties, evaluation, and results.

Elastomeric Insulator

The fabrication of elastically stretchable bilevel metallization requires two insulators: the PDMS substrate and an interlevel dielectric. The interlevel dielectric needs to be elastically stretchable, bond well with the underlying substrate, and be patternable so that openings can be made to form electrical connections (vias) between the two levels of metal. In addition, the via sidewalls need to be sloped to minimize the stress on the gold conductor when strained. The photopatternable silicone (PPS) WL5150 from Dow Corning fulfills all these

requirements. Table I compares the material properties of PPS, PDMS, and gold.

Nevertheless, combining PDMS and PPS for bilevel metallization poses several challenges. Both materials expand thermally and must be bonded temporarily to a glass slide during circuit fabrication. Also, while isopropyl alcohol (IPA) is the solvent of choice for rinsing PPS after patterning, PDMS swells when exposed to isopropyl alcohol. The layer thickness of PPS as an interlevel dielectric is also critical. Metal deposited on PPS layers that are too thin loses electrical continuity when stretched. We developed a fabrication process that addresses these challenges.

EXPERIMENTAL PROCEDURES

Fabrication of Test Structures for Elastomeric Bilevel Metallization

The test structure for our bilevel metallization consists of two gold layers,⁹ one on the PDMS substrate and the other on the PPS interlevel dielectric. Both layers are connected through via holes in the PPS dielectric (Fig. 1d, 1e). The geometry presented in Fig. 1 was designed so that a single structure could be used to individually examine bottom- and top-level metals and electrical connections between the two levels.

The preparation of the PDMS substrate (Fig. 1a) and the deposition and patterning of the bottom-level gold (Fig. 1b) were carried out as previously described.⁷

The PPS was spun on at 500 rpm for 30 s, providing a thickness of $55 \mu\text{m}$ (Fig. 1c). The remainder of the processing was carried out as previously described.⁷ Two steps in the fabrication discussed in Ref. 7 helped overcome the processing challenges associated with combining PDMS and PPS for bilevel metallization. First, a low processing temperature (90°C) was used when patterning the bottom-level gold by photolithography in order to minimize thermal expansion of the PDMS during this step. Second, the PPS was rinsed with IPA while being spun at 2,000 rpm to minimize exposure of the underlying PDMS to IPA. The top-level Au conductors, which formed the connections to the bottom-level metal (Fig. 1d, 1e), were e-beam evaporated through a steel foil shadow mask placed on top of the PPS. After removing the shadow mask, individual samples of the two-level conductors were

Fig. 1. Bilevel metallization fabrication process: (a) spin PDMS on a self assembled monolayer-coated glass slide; (b) deposit bottom metal stack of Cr/Au/Cr by e-beam evaporation and oxygen plasma etch metal surface; (c) spin PPS interlevel dielectric and create vias; (d) deposit top metal stack of Cr/Au by e-beam evaporation through steel foil shadow mask; (e) top view.

cut by hand with a razor blade and then peeled away from the glass slide.

Evaluation of the Test Structures

To understand the morphology of the conductors, the bottom- and top-level metals were examined by optical microscopy before and after the samples were strained by 30%. The via depth and shape were profiled to evaluate the topography of the via sidewalls, which affect the structure and electrical conductance of the metal connections between the top and bottom levels. To obtain this profile, PPS on a glass slide was patterned with via holes. Then a KLA Tencor profilometer—using a mass of 1 mg, scan speed of 20 μm/s, and sampling rate of 5 Hz—was used to measure the step height in the via hole from the glass to the top of the PPS. Because the via is merely a hole in the PPS layer, the PPS step height and via depth are equivalent. The PPS sidewall slope was measured on glass instead of on PDMS because PDMS is soft. When transitioning from PPS to PDMS, the surface profilometer tends to indent the PDMS and provide an inaccurate step height measurement of the PPS. Finally, we inspected the exposed top- and bottom-level

metals and the metal coverage of the vias using scanning electron microscopy.

We evaluated the electrical resistance of our bilevel metals under strain. The objective of this evaluation was to determine if individual metal layers and metal connections between layers remain electrically continuous when the entire structure is stretched. A custom-made stretcher⁹ was used to uniaxially stretch and relax the metal lines between 0% and 30% strain. The strain (ϵ) is defined as the change in length (ΔL) divided by the initial length (L), as shown in Eq. 1.

$$\epsilon = \frac{\Delta L}{L}. \quad (1)$$

Electrical connections were made to the metal lines by using silver paste to stick gold wires to both ends of the line. The contact points and the distances between the points are indicated in Fig. 1e. Two small pieces of PDMS on top of the silver paste held the gold wires in place. Electrical resistance was measured as a function of strain for bottom- and top-level metals. The metal lines were fabricated with different geometries to facilitate creating a single test structure that could be used to

Fig. 2. Normalized electrical resistance of conductors during one cycle of stretching and relaxation to a maximum of 30% uniaxial tensile strain. Cross-section schematics show the positions and dimensions of the samples that were measured.

individually examine bottom- and top-level metals and electrical connections between the two levels. As shown in Fig. 2, the bottom-level metal line was 7 mm long and 3 mm wide (sample A). The top-level metal line was 5 mm long and 1 mm wide (sample B). Electrical continuity between the two levels was also measured by contacting the top metal between two points that were 6 mm apart and connected through vias (sample C). For comparison, the electrical resistance of a separate structure, a single layer of Au on PDMS, was measured under strain as well, using a 7-mm-long 3-mm-wide metal line (sample D).

RESULTS

Bilevel Metallization Electrical Resistance and Morphology under Strain

We measured the electrical resistance of all samples in the relaxed state (initial resistance R_0) and under 30% uniaxial strain (Table II). Then we plotted the resistances R , during a complete cycle of straining and relaxation, normalized to the initial resistances, R_0 (Fig. 2). Top- and bottom-level metals and via connections between levels remained electrically continuous when strained by up to 30%

and when relaxed back to 0%. As summarized in Table II, the resistance increase was largest for electrical connections between the two levels (sample C). The top-level conductor (sample B) displayed the smallest resistance increase. The resistance of the bottom-level metal (sample A) increased just slightly more than that of the single-level sample (sample D).

Before the sample was stretched, both top and bottom metal films were continuous when inspected under the optical microscope (Fig. 3c). After the sample was stretched by 30%, both metal layers were cracked (Fig. 3d). As the substrate lengthened upon stretching, both metal layers formed cracks perpendicular to the stretching direction. However, the bottom metal layer also formed cracks during stretching that were parallel to the stretching direction, which are caused by Poisson compression of the substrate. The top metal layer did not display cracks parallel to the stretching direction. We profiled a bare via hole in the PPS that was peeled off the PDMS immediately after fabrication. This profile (Fig. 4) helped understand how the via sidewall might affect electrical connections between metal layers. The profilometer stylus was placed inside the via hole

Table II. Dimensions and electrical resistance of the one-dimensional (1D) conductors of Fig. 2

Conductor Sample	Description	Length (mm)	Width (mm)	Initial Resistance, R_0 (Ω)	Resistance at 30% Strain (Ω)
A	Bottom-level conductor	7	3	4.5	13
B	Top-level conductor	5	1	9	17
C	Conductor containing two via connections	6	1	30	135
D	Single-layer conductor	7	3	7	19

Fig. 3. (a) Side-view drawing of bilevel metallization as in Fig. 1. (b) Top-view drawing of bilevel metallization as in Fig. 1. (c) Optical micrographs of top and bottom metals before being stretched by 30% strain. (d) Optical micrographs of top and bottom metals after being stretched by 30% strain.

Fig. 4. Step height measurement and profile of PPS via, showing the slanted sidewall. The sample is a delaminated layer of PPS, with metallization, that is placed on a glass slide for profiling. The bottom of the profile is the glass surface. The raised shoulder is an artifact (see text).

on the glass slide and then scanned from the glass slide to the PPS substrate. The vias were approximately $55\text{ }\mu\text{m}$ deep with sidewalls that sloped over a $30\text{ }\mu\text{m}$ scan length (a slope of approximately 1.8). Even though the surface profiler indicated $15\text{-}\mu\text{m}$ -thick protrusions at the top edge of the sidewalls, no such protrusions were observed by scanning electron microscopy (SEM). Furthermore, this protrusion was only observed when the stylus moved up the sidewall but not when the stylus moved down the sidewall. Therefore we concluded

that the protrusion was an artifact of the surface profiler and not part of the PPS structure.

Top- and bottom-level metals and metal coverage of a via just after fabrication were studied by SEM (Fig. 5). The Au film completely covered the via sidewall. The top metal (Fig. 5e), bottom metal (Fig. 5d), and sidewall metal (Fig. 5c) immediately after fabrication all contained cracks, which resulted from peeling the sample off the glass slide.

DISCUSSION

The bilevel metallization remained electrically continuous during straining up to 30% and during relaxation. Previous works have shown that the Au films contain micrometer-sized cracks. These cracks enable the metal to stretch elastically while maintaining electrical conduction. The cracks allow the film to elongate by twisting out of plane, so that even at large elongation, only a small, elastic strain is induced in the film.¹¹

While microcracks enable the conductors to stretch elastically, they also cause the measured resistance of the conductors to be higher than the resistance¹⁰ calculated from the resistivity, ρ , of bulk gold:

$$R_{\text{bulk}} = \frac{\rho l}{wh}, \quad (2)$$

where l is the nominal length, w is the nominal width, and h is the thickness of the Au film.

The variation of the measured resistance R with strain ε (Fig. 2) shows three distinct regimes. The resistance of the top gold layer of the bilevel metallization (sample B) varies the least with strain. In this layer, the gold is bonded to the PPS. Under the optical microscope, the top gold layer also showed the fewest cracks after straining. These cracks formed in the metal during stretching and are larger than the cracks that formed in the metal when the sample was removed from the glass backing. The increase in the resistance with strain is larger when the gold conductor is bonded to PDMS, regardless of whether the gold is sandwiched between PDMS and PPS (sample A) or only bonded to PDMS (sample D). Sample C, which includes two via connections, varies the most and is quite noisy. This we ascribe to reduced and possibly nonuniform sidewall coverage caused by the off-normal angle of incidence during Au evaporation. Sidewall engineering could significantly increase sidewall metal coverage, thereby reducing the noise and resistance. After the first cycles of straining and relaxing, which are shown in Fig. 2, the relaxed resistances of samples A, B, and D were lower than the initial resistances R_0 . We commonly observe such reductions during the initial cycles of strain and relaxation. Upon investigating this phenomenon, we observed that the gold in microcracked samples often overlapped when relaxed. This overlap could increase the cross-section of the sample and reduce the resistance.

Fig. 5. Scanning electron micrographs of bottom metal, top metal, and metal on via immediately after fabrication: (a) overall structure, (b) magnified view of sidewall and vicinity, (c) metal on via sidewall, (d) bottom metal layer, and (e) top metal layer.

Since both top- and bottom-level metals remain electrically continuous when stretched, circuit components can be built on each layer of the structure and the bilevel metallization can serve as interconnects between components. However, when the bilevel metallization is stretched, the resistance of Au on PDMS increases more than the resistance of Au on PPS. This is likely because PPS is less compliant than PDMS, as indicated by comparing the Young's moduli of the two materials (Table I). Au patterned on the softer PDMS cracks more and displays a greater increase in resistance than Au patterned on the stiffer PPS. Therefore, conductors on the PPS layer could serve as interconnects for devices that require a smaller increase in resistance. Circuit models should account, and designs should compensate, for the larger resistance increase of conductors connecting the two metal layers through via holes.

The additive nature of fabrication (Fig. 1) and the preceding electrical results suggest that our bilevel metallization technology can be further developed to fabricate multilevel metallization. Since PPS is a suitable interlevel dielectric for two metal layers, it could also serve as the dielectric for multiple metal layers.

The bilevel metallization technology that we developed is suitable for fabricating stretchable circuits that cannot be created with planar, single-level, metallization alone, as we now demonstrate.

APPLICATION

An Elastically Stretchable *RLC* Circuit

We used our elastically stretchable bilevel metallization technology to fabricate a stretchable *RLC* resonant circuit. An *RLC* circuit's impedance is a function of the frequency of an AC source. The magnitude of the impedance is greatest at the frequency where the inductive and capacitive components are equal.¹³ The resonance frequency of the stretchable *RLC* circuit changes as the circuit is strained because the geometries of the inductor and capacitors change with strain. We stretched the *RLC* circuit in two dimensions simultaneously, because in contrast to the 1D interconnects, both the inductor and the capacitors are two-dimensional (2D) devices. The biaxial strain is the change in length divided by the initial length and the change in width divided by the initial width. Both length and width were changed by equal amounts, so that $\varepsilon = 3\%$ biaxial strain, for example, represents a simultaneous 3% increase in length and a 3% increase in width.

The inductance L of a planar square spiral inductor is approximated well by the expression¹⁴

$$L \cong \mu_0 a_{\text{avg}} [K_1 n^2 / (1 + K_2 \rho)], \quad (3)$$

where μ_0 is the permeability of free space, a_{avg} is the average length of the longest and the shortest sides

Fig. 6. (a) Schematic top view of the stretchable *RLC* circuit; dimensions in mm. (b) Cross-sectional view.

of the square spiral, K_1 and K_2 are parameters that are constant for the square layout, n is the number of turns of the spiral ($n = 2$, see Fig. 6), and ρ is the fill ratio of the inductor. The fill ratio ρ is the difference between the longest and the shortest side lengths divided by their sum. All of these parameters except for a_{avg} remain constant during 2D stretching. With

$$a_{\text{avg}}(\varepsilon) = a_{\text{avg}}(\varepsilon = 0)(1 + \varepsilon), \quad (4)$$

the inductance L of the planar spiral will depend on strain as

$$L(\varepsilon) \cong L(\varepsilon = 0)(1 + \varepsilon). \quad (5)$$

The capacitances associated with the spiral inductor are dominated by the two Au/PPS/Au capacitors (Fig. 6). Their parallel-plate capacitance C is given by

$$C = \epsilon_r \epsilon_0 A/h, \quad (6)$$

where ϵ_r is the relative dielectric constant of PPS (Table I), ϵ_0 is the permittivity of free space, A is the surface area of the capacitor plates, and h is the thickness of the PPS. Of these parameters, A and h vary with 2D stretching to biaxial strain ε as

$$A(\varepsilon) = A(\varepsilon = 0)(1 + \varepsilon)^2, \quad (7)$$

and, because of volume conservation during the deformation of an elastomer,

$$h(\varepsilon) = h(\varepsilon = 0)(1 - \varepsilon)^2. \quad (8)$$

Therefore, the capacitance C varies with 2D stretching to strain ε in both x and y directions as

$$C(\varepsilon) = C(\varepsilon = 0)(1 + \varepsilon)^4. \quad (9)$$

The resonant frequency f_0 of the inductor circuit is given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \quad (10)$$

Substitutions from Eqs. 5 and 9 into Eq. 10 shows that the resonant frequency varies with 2D stretching by strain ε approximately as

$$f_0(\varepsilon) \cong f_0(\varepsilon = 0) / (1 + \varepsilon)^{5/2}. \quad (11)$$

Circuit Design and Fabrication of the Elastomeric *RLC* Circuit

The planar stretchable *RLC* circuit (Fig. 3) contains one 9 mm × 11 mm capacitor in the center (C_1) and one 12 mm × 11 mm cross-over capacitor (C_2). The top and bottom capacitor plates are connected by a planar, square spiral inductor (L). The circuit was made by e-beam evaporating a 125-nm-thick bottom Au layer (with 3 nm of Cr below and above for adhesion) onto a 300-μm-thick PDMS substrate. The bottom Au layer was patterned by photolithography to form the inductor and bottom capacitor plates. Then a 55-μm-thick PPS interlevel dielectric was spun on top of the Au and patterned by photolithography to open 1 mm × 1 mm vias. Finally, a 125-nm-thick Au layer (with 3 nm of Cr for adhesion) was e-beam evaporated on top of the PPS through a Dupont Kapton® E foil shadow mask to form the top capacitor plates and the via connection to the bottom metal layer. The Au film thickness was increased to 125 nm (from the 75 nm that we used for the interconnects) to decrease its electrical resistance. A disadvantage of 125-nm-thick films is that they become electrically open at smaller strains than 75-nm-thick films.

Evaluation of Relaxed and Strained *RLC* Circuit

We measured the circuit's impedance in the relaxed and stretched states as a function of AC frequency. An AC voltage source was connected to the series combination of a 10 Ω test resistor (R_{test}) and the *RLC* circuit (Fig. 7). Electrical connections were made to the circuit by using silver paste to stick gold wires to the inductor and the top plate of capacitor C_1 as shown in Fig. 7. Two small pieces of PDMS held the gold wires in place. First, an ohmmeter was connected to these gold wires, and the direct-current (DC) resistance of the Au inductor was measured. Then a Keithley 2000 digital multimeter was used to measure voltage drops across the *RLC* circuit (V_Z) and the test resistor (V_R) as the frequency was stepped from 35 MHz to 55 MHz in 1 MHz increments. Equation 12 was then used to extract the magnitude of the circuit's impedance as a function of frequency.¹⁵

$$|Z| = \frac{V_Z}{V_R} R_{\text{test}}. \quad (12)$$

Fig. 7. Setup used to measure the magnitude of the stretchable circuit's impedance: (a) drawing of physical setup; (b) equivalent circuit.

After measuring the impedance of the relaxed circuit, the circuit was biaxially strained by 1%, 3%, and 6%. One corner of the circuit was first clipped to a glass slide. Next, the circuit was stretched in the X-direction by the desired amount and clipped in place. Finally, the circuit was stretched in the Y-direction by the desired amount and clipped in place. The impedance and DC resistance were measured at each strain value. After stretching to 6% strain, the circuit was relaxed, and the impedance and DC resistance were measured again at 0% strain. The measured resistances R are listed in Table III. The measured impedance magnitudes are plotted in Fig. 8 as functions of frequency for the circuit before straining, for 1%, 3%, and 6% biaxial strain, and again at 0% strain. The maximum impedances $Z(f_0)$ and the corresponding resonant frequencies f_0 also are listed in Table III.

The quality factor Q was calculated from the measured impedance–frequency characteristic by dividing the circuit's resonant frequency (f_0) by the bandwidth of its AC response (Eq. 13). The bandwidth, B , is the difference between the two frequencies at which the impedance magnitude decreases from its maximum value at f_0 to 0.707 of that value.

$$Q = \frac{f_0}{B}. \quad (13)$$

The calculated values of Q also are entered in Table III.

DISCUSSION

Figure 8a–8e and Table III suggest that f_0 decreases approximately linearly with increasing

biaxial strain, ε . Increasing ε by 1% reduces f_0 by approximately 1 MHz. Figure 8f shows that f_0 decreases linearly with $(1 + \varepsilon)^{5/2}$ as expected from Eq. 11. Approximate linearity in both ε and $(1 + \varepsilon)^{5/2}$ is not surprising because the values of ε are sufficiently small to allow termination of the linear expansion of $(1 + \varepsilon)^{5/2}$ after two terms, as

$$(1 + \varepsilon)^{5/2} \cong 1 + (5/2)\varepsilon. \quad (14)$$

The circuit's maximum impedance $Z(f_0)$ increases and the quality factor Q decreases with rising strain. The circuit's R and even more so its Z increase with ε much more strongly than anticipated from the evaluation of the 1D stretching of interconnects. This result is not surprising because the electrical continuity of the Au film is affected differently by 1D or 2D stretching. One-dimensional stretching separates segments of the film along the stretching (x) direction, but pushes them into each other in the y direction as a consequence of Poisson compression. Two-dimensional stretching separates film segments in both x and y directions. The RLC circuit results motivate a detailed study of the electrical conductance under slow 2D stretching, for both bare and encapsulated metallization.

CONCLUSIONS

The developed elastically stretchable bilevel metallization maintained its electrical continuity when stretched by up to 30% uniaxial strain. This bilevel metallization was used to fabricate a stretchable RLC circuit that contained two capacitors and a square planar inductor. The RLC circuit remained electrically conducting when stretched by up to 6% biaxially. Its resonant frequency dropped

Fig. 8. The magnitude of the *RLC* circuit's impedance as a function of frequency f and 2D strain ϵ , evaluated (a) before straining, at (b) 1%, (b) 3%, and (d) 6% biaxial strain, and (e) when relaxed to 0% after straining. The impedance peaks at the circuit's resonant frequency, which decreases with increasing strain. (f) Resonant frequency f_0 plotted versus $(1 + \epsilon)^{5/2}$.

Table III. Resonant frequencies and quality factors of the stretchable *RLC* circuit as functions of 2D strain values

Biaxial Strain ϵ (%)	Resistance R (Ω)	Maximum Impedance $Z(f_0)$ (Ω)	Resonant Frequency f_0 (MHz)	Quality Factor Q
0 (before strain)	14	113	47	5.9
1	17	565	46	5.1
3	31	1600	44	4.9
6	60	3636	41	4.1
0 (after strain)	15	125	47	5.9

approximately linearly with increasing biaxial strain. The *RLC* circuit successfully demonstrated elastically stretchable bilevel metallization, with the reservation that the quantitative modeling of $Z(f)$ and of Q awaits quantification of the electrical response of the conductors to 2D stretching. The next step in application will be to go from bilevel to multilevel metallization, for the purpose of demonstrating an elastomeric wiring membrane.

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