Journal of Real-Time Image Processing: fourth issue of volume 8

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Published online: 14 November 2013
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The fourth issue of volume 8 completes another successful year of JRTIP publication by having received and reviewed a high volume of manuscript submissions. This trend exhibits a steady increase of real-time importance as related to image and video processing. Real-time image and video processing technologies demand co-designs of software with reduced complexity and their adaptation to appropriate hardware platforms which normally possess limited resources. JRTIP continues to be the only journal that is solely dedicated to the real-time aspects of image and video processing spanning a wide range of industrial and R&D applications. The special issues organized thus far have also greatly demonstrated the real-time focus of JRTIP through offering modern topics of interest to the real-time image and video processing community.

The ongoing success of JRTIP is reflected by an increase in its 2012 impact factor to 1.156 (Thomson Reuters Journal Citation Reports® 2012). Many have contributed to this increase. First and foremost, we would like to express our appreciation to the JRTIP dedicated team of associate editors for their handling of manuscripts. Our thanks extend to authors and reviewers for submitting manuscripts and for reviewing manuscripts, respectively. In addition, we wish to acknowledge our growing community of readers who have downloaded 25,000+ JRTIP articles.

Of course with success come challenges. One of the challenges has been coping with the increasing number of

submitted manuscripts. To address this challenge, we invited the guest editors of the recent special issues as well as experienced researchers to join the editorial board. These colleagues have become familiar with the quality standards practiced by the journal, and the issues associated with its reviewing process through their successful offerings of special issues and other interactions with the journal. As a result, we are delighted to welcome the following colleagues to the JRTIP editorial board: Luis Alvarez, Daniel Chillet, Marco Diani, Michael Hübner, Bogdan Smolka, Leonel Sousa, and Juan Wachs.

Another challenge accompanying the success of JRTIP has been the relatively long list of accepted manuscripts on Online First that are to appear in print format. To address this challenge, we are pleased to indicate that the number of pages will be increased from 320 to 640 pages per year. That is to say starting with volume 9 in 2014, on average, twice as many papers will appear in the four annual volumes of JRTIP. We are thankful to Springer for providing the required resources to double the number of print pages.

Before providing an overview of papers appearing in this issue, it is worth reminding our readers of the upcoming SPIE Conference on Real-Time Image and Video Processing that is going to be held as part of the SPIE Photonics Europe in April 2014 in Brussels, Belgium. Similar to the previous years, the JRTIP editorial board will be meeting and discussing the status of the journal at this conference. The conference details are available at <http://www.spie.org/epe115> and its call for papers appears as an appendix to this issue.

This issue presents seven original research papers that reflect the real-time thrust of the journal indicating different ways real-time image and video processing can be achieved, where three papers address algorithmic real-time solutions and four papers address hardware real-time solutions.

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The first paper by Paul et al. describes a hexapod walking rescue robot named OSCAR which is capable of detecting motion in real-time by a single camera. The solution provided deals with strong rotation and translation in 3D with four degrees of freedom where slow and fast moving objects are detected using a histogram-based vector clustering and a motion compensated frame differencing. This approach is shown to provide improvement over the previous techniques. The FPGA implementation reported can process video frames in real-time at 31 fps.

The second paper by Zemčik et al. describes an algorithm designed for correction of small geometrical distortions introduced by optical devices in real-time. Displacements in the range of few pixels are corrected by high sub-pixel precision via bi-linear interpolation within each node of a rectangular mesh. Beside the algorithmic aspects, the paper also discusses the FPGA implementation aspects of this geometric correction algorithm.

The third paper by Ishii et al. discusses a high-speed vision system for real-time face tracking on a GPU processor. Based on the Viola-Jones face detector, face tracking is accelerated by reducing the number of window searches for Haar-like features where the tracked face pattern, in cases the window is sparsely scanned, can still be localized pixel-wise by incorporating a skin color extraction in the detector. The implementation on a GPU-based vision platform is shown to achieve face tracking of approximately 500 fps.

The fourth paper by Genovese et al. addresses an FPGA architecture for real-time segmentation and de-noising of HD video. The segmentation is achieved based on a Gaussian mixture model and the de-noising is achieved via a set of morphological filters. The real-time demand is defined in terms of the speed and size of HD video sequences ($1,920 \times 1,080$ @ 20 fps). The optimized fixed width representation of the data implemented on Xilinx and

Altera FPGAs allows processing 24 fps of HD video using 1179 slice LUTs and 291 slice registers with a dynamic power dissipation of 0.46 mW/MHz.

The fifth paper by Wahid et al. describes an efficient hardware implementation of cosine transform for video coding. This is driven by the demands of several video decoders to support multiple video standards, such as H.264/AVC, JPEG, MPEG-2/4, VC-1, and AVS, on a single platform. This is realized by a cost-sharing architecture based on a multi-dimensional delta mapping to allow multiple transforms for all five video codecs. The inverse transform matrix of the discrete cosine transform (DCT) of AVS having the lowest computational complexity is used to compute the inverse DCT matrices of the other four codecs. The proposed architecture uses only shared adders and shifters, which allow reducing the hardware complexity considerably.

The sixth paper by Lucking et al. is thematically related to the fifth paper as it discusses an FPGA implementation of the JPEG2000 MQ decoder as a flexible binary arithmetic decoder to reduce the amount of FPGA resources used leading to 19 % more entropy block decoding and increasing the throughput by 21 % over previous designs.

The final paper by Hosseini et al. deals with a fast implementation of a class of dense stereo vision algorithms. The implementation is done on a low power massively parallel SIMD architecture. Two cores, each consisting of 96 processing elements, provide a peak processing rate of 96 GFLOPS at low power consumption. A parallel implementation for the sum of squared difference (SSD) algorithm operating on VGA resolution images with disparity ranges of 16 and 32 is shown to achieve a processing rate of 179 and 94 fps, respectively. HDTV images with disparity ranges of 16 and 32 are processed at 67 and 35 fps, respectively.