Special issue (part III) on parallel computing for real-time image processing

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The performance requirements of image processing applications have continuously increased, especially when they are executed under real-time constraints. We have organized this special issue on *Parallel Computing for Real-Time Image Processing* to present the current state-of-the-art in the field of parallel programming and the future trends in real-time image and video processing as related to parallel computing or real-time implementation of embedded image processing applications on parallel architectures including multi-core platforms, GPUs and dedicated parallel architectures based upon FPGAs.

Due to the overwhelming number and their wide scope of submissions received for this special issue and thus the difficulty associated with finding expert reviewers, it was decided to offer this special issue in three parts. We are very grateful to the reviewers who provided valuable comments and suggestions to improve the quality of the accepted papers.

This third part of this special issue on *Parallel Computing for Real-Time Image Processing* presents five papers addressing different parallel applications including 2D wavelet transform, tone mapping, object recognition, face tracking and dynamic video applications. The real-time implementation of these applications uses GPU, parallel multi-core architecture and dedicated architecture based upon FPGA. Brief outlines of these papers are stated below:

The first paper by Franco et al. presents a GPU implementation of the 2D Fast Wavelet Transform, based on a pair of Quadrature Mirror Filters. It also investigates hardware improvements including multicores on the CPU side, and exploits them at thread-level parallelism using OpenMP and Pthreads. Overall, the GPU exhibits better scalability and parallel performance on large-scale images to become a solid alternative for computing the 2D-FWT versus those thread-level methods run on emerging multi-core architectures.

The second paper by Liu et al. proposes a multi-cue-based face tracking algorithm with the supporting framework using parallel multi-core and one graphic processing unit (GPU). This paper explores two parallel computing techniques to speed up the tracking process, especially the most computation-intensive observational steps. One is a multi-core-based parallel algorithm with a Map-Reduce thread model, and the other is a GPU-based speedup approach. The GPU-based technique uses features-matching and particle weight computations, which have been put into the GPU kernel. The results demonstrate that the proposed face tracking algorithm can work robustly with cluttered backgrounds and differing illuminations; the multi-core parallel scheme can increase the speed by 2–6 times compared with that of the corresponding sequential algorithms. Furthermore, a GPU parallel scheme and co-processing scheme can achieve a greater increase in speed (8x–12x) compared with the corresponding sequential algorithms.

The third paper by Akil et al. presents the parallel implementation on a GPU of a Real-Time Dynamic Tone Mapping Operator. It describes a generic operator that may be used by any application. However, the goal of this work is to integrate this operator into the graphic rendering process of a car driving simulator, based on its real-time implementation. The tone mapping operator outputs a low

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dynamic range (LDR) image keeping as much as possible the contrast and luminance of the original input high dynamic range (HDR) image. It performs the mapping between the luminances of the original scene and the output device's display values. This paper addresses the problem of mapping HDR images to standard displays. In this case, the tone mapping compresses the luminances ratio. Several tone mapping operators can be found in the literature as well as some parallelizations. However, they use either static or adaptations of static operators. The dynamic operator of Irawan is adapted and parallelized on the GPU Nvidia 8800 GTX (728 MB, 518GFLOPS). The execution speed has been increased by a factor of 15 compared to a straightforward implementation of the algorithm. The display rate reaches 30 images per second, which fulfills the real-time video rate of 25 images per second.

The fourth paper by Cao et al. proposes a buffering scheme suitable for implementing real-time vision-based systems on an FPGA that does not require external memory to buffer data. A stop sign detection system implemented on an FPGA employing the proposed buffering scheme is presented as an example. This system is capable of processing over 200 fps at the frame size of 480×752 pixels.

The final paper by Albers et al. addresses the efficient mapping and reconfiguration of advanced video applications onto a general purpose multi-core platform. By accurately modeling the resource usage for an application, allocation of processing resources on the platform can be based on the actually needed resources instead of a worst-case approach, thereby improving quality-of-service (QoS).

This paper exploits a new and strongly upcoming class of dynamic video applications based on image and content analysis for resource management and control. Such applications are characterized by irregular computing behavior and memory usage. It is shown that with linear models and statistical techniques based on Markov modeling, a rather good accuracy (94–97 %) for predicting the resource usage can be obtained. This prediction accuracy allows resource prediction at runtime, thereby leading to an actively controlled system management.

Author Biographies

Mohamed Akil received his PhD degree from the Montpellier University (France) in 1981 and his doctorat d'état from the Pierre et Marie Curie University (Paris, France) in 1985. He currently teaches and does research with the position of Professor at Computer Science Department, ESIEE, Paris. He is a member of Institut Gaspard-Monge, unité mixte de recherche CNRS-UMLPE-ESIEE, UMR 8049. His research interests are architecture for image processing, image compression, reconfigurable architecture and FPGA, high-level design methodology for multi-FPGA, mixed architecture (DSP/FPGA), system on chip (SoC) and parallel programming of 2D/3D topological operators. Dr. Akil has more than 80 research papers in the above areas.

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