Editorial

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The newest family of H.264 video coding standards (AVC, SVC, and MVC) have shown great rate distortion performance improvements compared to the MPEG-2/MPEG-4 standards. The improvements come from the use of multiple reference frames, multiple intra prediction modes, motion estimation with variable block sizes, quarter-pixel accuracy, integer cosine transform and Context-adaptive binary arithmetic coding (CABAC). However, these improvements impose a high computational cost, which makes the implementations of this family of standards challenging for real time applications. In this special issue, a variety of algorithmic and micro-architectural optimisations are proposed for reducing the computational cost while retaining the rate distortion performance of the standards at acceptable levels. The issue consists of nine papers and the remainder of this editorial presents a brief summary for each of them.

In the paper, “Low complexity quantization for H.264 AVC”, Jiang et al. present a novel hardware based quantization scheme, where large bit width of multipliers in H.264 AVC are substituted by a set of small bit width adders. The quantization error induced by this process is both theoretically but also experimentally investigated. The proposed hardware modification results in significant power and area savings in the area of VLSI design, while the rate distortion performance is only negligibly degraded.

In the paper, “Fast adaptive termination mode selection for H.264 scalable video coding”, Ren and Kehtarnavaz present a three-stage method for fast adaptive termination

in the mode decision phase of the coding pipeline. The first stage consists of a predictive step based on the rate distortion costs of neighboring and collocated macroblocks. The second stage uses the derivation of a modulation factor and the results of stage one in order to form an adaptive rate distortion threshold against which a subset of modes is compared in a specific order to facilitate early termination. The second stage is similar to stage one for the remaining modes and operates both on the base and enhancement layers. The proposed method provides close to one-third reduction in the computation requirements as compared to the high complexity mode of H.264 SVC with negligible degradation in the rate distortion performance.

In the paper, “HDS, A Real time multi-DSP motion estimator for MPEG-4/H264 AVC High definition video encoding”, Urban et al. propose a Hierarchical Diamond Search (HDS) motion estimation scheme which is a trade-off between Enhanced Predictive Zonal Search (EPZS) and Hierarchical Motion Estimation (HME). The proposed technique achieves a balance between computational complexity and rate distortion performance. It is applicable in multi-core DSPs and is particularly relevant to high definition video.

In the paper, “Real time Data hiding by exploiting the IPCM macroblocks in H.264 AVC streams”, Kapotas and Skodras present a fragile and blind data hiding technique. The method is applicable to IPCM encoded macroblocks produced in the intra mode decision phase of the H.264 AVC, embeds data in pixel domain and achieves real time performance. It further has the useful property of allowing multiple reuse of the compressed bit stream for data hiding without significant degradation of the rate distortion performance. The proposed scheme suits covert communication and content authentication applications.

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In the paper, “Architecture of an Application Specific Processor for Real-time Implementation of H.264/AVC Sub-pixel Interpolation”, Dang presents an efficient VLSI architecture for sub-pixel interpolation in the motion estimation phase of the H.264 AVC standard. In the proposed scheme, many different optimization techniques are utilised in a variety of micro-architectural levels, such as parallel processing, vector registers, pipelined architecture and in-place computation. These techniques result in reduction of the number of memory accesses and acceleration of interpolation computations, thus making the processor architecture capable of calculating sub-pixel interpolations for a 16×16 luminance macro blocks in 84 clock cycles. The proposed optimizations are ideal for portable devices running at low clock rates to save power.

In the paper, “Accelerating the multiple reference frames compensation in the H.264 video coder”, Hachicha et al. deal with the problem of reducing the computational and memory bottlenecks caused by multiple reference frames in H.264 AVC. These frames despite improving the rate distortion performance for sequences containing uncovered backgrounds, repetitive motions and highly textured areas, they make the realisation of the standard problematic for mobile devices. The authors propose a robust Markov Random Field (MRF) algorithm for motion segmentation, which enables the decrease in the number of default reference frames needed in H.264 AVC from five to three for very similar rate distortion performance. Computational savings in the order of 35% are reported as a result of fewer reference frames.

In the paper, “Real-time Interactive Regions of Interest in H.264/AVC”, Lambert et al. show two methods for adaptively changing at decoding time the size and position of the coded Regions of Interest (ROIs). Both methods rely on the Flexible Macroblock Ordering (FMO) concept, which despite initially being used for error resilience, it has also found applications in region of interest coding. The first method allows for change of the size of the output video pane in order to better match decoder displays, while the second method makes it possible to select a ROI at run time without the need for an encoder to provide the ROI

specification in the bit-stream. Both approaches allow for real time adaptation of the H.264 AVC bit-stream and can achieve significant bit rate savings. Furthermore, they can speed up decoding while maintaining the bit rate overhead controllable.

In the paper, “Real-time Error Concealing Bit-stream Adaptation Methods for SVC in IPTV Systems”, Lambert et al. present an adaptation method in H.264 SVC which enables concealment of bit-streams while at the same time allowing them to remain SVC compatible. The method is exactly equivalent to a passive concealment strategy performed at the decoder end. The proposed technique produces decoded sequences with significantly higher visual quality than the standard and does not require any modification to SVC compliant decoders. Furthermore, it is extremely fast (more than 900 fps) and produces negligible bit-rate overheads (around 0.2%).

Finally, in the paper “An improved rate control algorithm based on a novel shot detection scheme for the H.264/AVC standard”, Grecos et al. firstly propose a novel MPEG-7 descriptor driven shot detection method with low computational cost for H.264/AVC. Then they exploit this scheme to determine the initial quantization parameters for each shot through modeling. These two steps can help reducing significantly the bit rate and PSNR fluctuations per shot in the case of multiple shot video sequences as compared to the rate control of the H.264/AVC.

This Special Issue has assembled a small sample of papers originating from well-known research groups worldwide. The contributing authors were instrumental in the completion of the Special Issue and the editor would like to thank each of them for their effort and for adhering to schedule deadlines. The editor would also like to thank the anonymous referees who played a key role in the review and selection process with their insightful comments, ensuring the Special Issue includes only the submissions of highest technical quality.

I hope you will enjoy this special issue.

Christos Grecos
Guest editor