A novel lambda negative-resistance transistor in the 0.5 μm standard CMOS process

CHEN Yan^{*}, MAO LuHong, GUO WeiLian, YU Xin, ZHANG ShiLin & XIE Sheng

School of Electronic Information Engineering, Tianjin University, Tianjin 300072, China

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A novel negative-resistance transistor (NRT) with a Lambda shaped I - V characteristic is demonstrated in the 0.5 μm standard CMOS process. To save on the number of component devices, this device does not use standard device models provided by CMOS processes, but changes a MOSFET and a BJT into a single device by fabricating them in the same n-well, with a p-type base layer as the MOSFET's substrate. The NRT has a low valley current of -6.82 nA and a very high peak-to-valley current ratio of 3591. The peak current of the device is $-24.49\text{ }\mu\text{A}$ which is low enough to reduce the power consumption of the device, and the average value of its negative resistance is about $32\text{ k}\Omega$. Unlike most negative-resistance devices which have been fabricated on compound semiconductor substrates in recent years, this novel NRT is based on a silicon substrate, compatible with mainstream CMOS technology. Our NRT dramatically reduces the number of devices, minimizing the area of the chip, has a low power consumption and thus a further reduction in cost.

lambda negative-resistance transistor, CMOS, p-base layer, peak-to-valley current ratio, low power consumption

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Negative-resistance transistors (NRTs) have been researched for nearly 100 years, and are types of devices with negative resistance characteristic, which means the slope of their I - V curve is negative in certain regions. NRTs have a vast potential in many types of digital logic gates and memory circuits [1–3], such as the high-density static RAM made by Wu et al. in 1983 [4], the D flip-flop by Cheng and Duane in 2006 [5], the static RAM by Chen et al. in 2009 [1] and the spin-torque-transfer (STT) magnetoresistive RAM made by Halupka et al. in 2010 [6], etc. More recently, there have been many other negative-resistance devices such as carbon nanotube negative-resistance devices [7], metal-insulator-metal diodes on insulating films [8,9], and the resonant tunneling diode which have attracted much attention and been demonstrated in III-V compound semiconductor substrates. However, these devices are not all compatible with standard CMOS technology [10]. A demonstration based on

CMOS technology would widen the application scope of the NRTs, but also reduce the processing difficulties and increase their manufacture rate. Therefore, a suitable Si-based negative-resistance device compatible with the CMOS process has become more and more interesting to circuit designers.

In this paper, a novel voltage-controlled NRT is presented. This device is designed and fabricated by using of the standard 0.5 μm CMOS process, mainly applied to digital logic circuits such as logic gates and RAMs. As is well known, the typical CMOS logic circuit is constructed by a number of MOS or BJT devices [11,12], for example a D flip-flop on CMOS technology is constructed using nearly 20 MOSFETs. One BJT and two resonant tunneling diodes could also form a D flip-flop, but could only be realized in a compound process. Under these conditions the novel NRT is the best choice because it needs only two NRT devices to displace the 20 devices and still be compatible with CMOS technology, dramatically reducing the number of devices

^{*}Corresponding author (email: chyan@tju.edu.cn)

and the area occupied. This characteristic is particularly evident when used in large-scale logic arrays [13]. The working current of the device is several tens of microamperes, which is quite low compared to most negative resistance devices. There are types of negative resistance devices that work under several milliamperes or more, such as silicon controlled rectifiers and voltage controlled oscillators. However, the device mentioned here is mainly used in digital logic circuits, where the smaller working currents result in lower power consumption, which is one of the most important parameters of the digital logic circuits.

The equivalent circuit of an NRT is shown in Figure 1(a) which employs an n-channel depletion MOSFET and a lateral pnp transistor [14]. There are three terminals in the NRT named the Base (B), Collector (C) and Emitter (E) terminals as shown in Figure 1(a). The source and substrate of the MOSFET are connected internally, working as the base terminal of the NRT. The drain of the MOSFET and base of the BJT are connected externally by metallization. The gate of the MOSFET and collector of the BJT are also connected externally by metallization, working as the collector terminal of the NRT. The emitter of the BJT still works as the emitter of the NRT and is grounded.

Both the base-emitter voltage (V_{BE}) and collector-emitter voltage (V_{CE}) of the NRT are fixed, with a negative bias voltage. The resistor R_C is used to modify the impedance of the device in the positive-resistance region. Figure 1(b) shows the basic structure of the NRT. Different from the common MOSFET and BJT structure of the standard CMOS process, the MOSFET is fabricated into the p-base layer which is typically the base region of an npn bipolar transistor. The p-base layer is also a p-type semiconductor

Figure 1 (a) Electrical equivalent circuit of the NRT; (b) basic device structure of the NRT.

material working as the substrate of the MOSFET. In this way the lateral pnp transistor and the MOSFET can both be fabricated into the same n-well, minimizing the total area of the NRT. Figure 2 shows the microphotograph of the NRT. The left part is the n-channel depletion MOSFET and the right part is the lateral pnp-BJT. To minimize the area occupied by the chip, the width to length ratio of the MOSFET gate is $20\ \mu\text{m}/2\ \mu\text{m}$, the base area of the lateral pnp transistor is $11.2\ \mu\text{m}^2$, the emitter and collector area of the lateral pnp transistor are both $15.4\ \mu\text{m}^2$, and the total size of the device is $21\ \mu\text{m} \times 23\ \mu\text{m}$.

The typical I_{CE}/V_{CE} characteristic of the NRT is shown in Figure 3(a) which was measured using a Keithley 4200 instrument at room temperature. As analyzed previously, the input base voltage V_{BE} and collector voltage V_{CE} are both fixed with a negative bias. The V_{CE} is from 0 to $-1\ \text{V}$, with a $-0.02\ \text{V}$ per step, while the V_{BE} is from 0 to $-2.5\ \text{V}$, with a $-0.1\ \text{V}$ per step.

It is well known that the negative resistance R_N equals the derivative of V_{CE} with respect to I_C , i.e. $R_N = dV_{CE}/dI_C$. R_N is positive when the curve of the I_C/V_{CE} is upward, and it is negative when the curve is downward. However, the value of R_N will not remain the same. The changes in R_N depend on the changes in the slope of the curve. For example, in Figure 3(a), when V_{BE} is $-2.5\ \text{V}$, the curve of I_C/V_{CE} is marked by two dotted ellipses, which represent the Negative-Resistance Region I and Region II respectively. The peak value of I_{CE} can be observed when V_{CE} is around $-180\ \text{mV}$. The average value of R_N is the ratio of the difference between the peak and valley value of V_{CE} divided by the difference between the peak and valley value of I_{CE} [15]. When V_{BE} is $-2.5\ \text{V}$, the average value of R_N is about $32\ \text{k}\Omega$. The figure shows that in Region I, the slope of the curve decreases as V_{CE} increases. Therefore the negative resistance decreases as V_{CE} increases; in Region II, the slope of the curve increases as V_{CE} increases. Therefore the negative

Figure 2 The device microphotograph enlarged 100 times showing the MOSFET and BJT in the same n-well.

Figure 3 (a) The I_{CE}/V_{CE} characteristic of NRT measured by Keithley 4200 (both the input voltage V_{CE} and input current I_{CE} are negative, with the $PVCR=3591$); (b) the relationship of R_N/V_{CE} when V_{BE} is -2.5 and -2.4 V (There are only two curves because when V_{BE} is less than -2.4 V, the value of R_N is too high and cannot change along the variation tendency as these curves do).

resistance increases as V_{CE} increases. The relationship of R_N/V_{CE} is shown in Figure 3(b). The variation tendencies of R_N in the Negative-Resistance Region I and II confirm the preceding analysis about the slope. The value of V_{CE} in the Negative-Resistance Region I and II is between -150 and -240 mV. The value of R_N drops dramatically when V_{BE} is higher than -240 mV.

The peak-to-valley current ratio is the ratio of the peak value of the current (I_P) divided by the valley value of the current (I_V) [15]. For example when V_{BE} is -2.5 V, I_P is $-24.49 \mu A$ and when V_{CE} is -180 mV, I_V is -6.82 nA when V_{CE} is -1 V. Therefore the $PVCR$ is about 3591, and high

enough for most digital logic circuits such as inverters and D flip-flops. The valley current is also an important parameter, which represents the value of the leakage current when the device is off. A -6.82 nA valley current is small enough for low power consumption.

In conclusion, we have designed and fabricated a novel lambda NRT in the $0.5 \mu m$ standard CMOS process. The equivalent circuit of the NRT is constructed using an n-channel depletion MOSFET and a lateral pnp-BJT. Both the devices are reconstructed into a single n-well and have the p-base layer as the substrate of the MOSFET, dramatically reducing the number of devices and the area occupied on the chip. The NRT successfully achieved the negative resistance characteristic with a very low valley current of -6.8217 nA and low power consumption. After analysis and calculation, the average value of R_N is about $32 k\Omega$ with a V_{BE} of -2.5 V. The NRT has a relatively high $PVCR$ of 3591 and is compatible with standard CMOS technology. It has huge potential value in digital logic circuits and RAM applications.

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