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Editorial

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Digital Signal Processing (DSP) architectures have emerged as considerable driving forces in consumer electronics, communications, entertainment, medical devices, video games, and computing in general. These technologies have gained, even, more significance due to the new developments in Internet and Wireless Communication, Portable Multimedia, Smart Sensors, and Cognitive Systems. As the demands of the market and consumers grew exponentially, new and key advanced technologies have to be developed in DSP algorithms, circuits, architectures, implementation, design methods, and prototyping. Implementation and Prototyping of DSP systems have become very sophisticated because of the increasing demands at each level and the market dynamics.

This special issue is focused on implementation and prototyping of DSP architectures for multimedia communications. Several case studies are given in various implementation technologies. It shows the impact of implementation technologies on the performance of a system. It also demonstrates the significance of prototyping on the success of the final product. The first three papers are case studies of prototyping in ASIC technologies. They are a demonstration of how to improve the system performance at the circuit level.

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The first paper, **Efficient 45 nm ASIC Architecture for Full-Search Free Intra Prediction in Real-Time H.264/AVC Decoder,** presents an ASIC architecture for a high throughput Full-Search Free (FSF) intra mode selection and direction prediction algorithm for H.264/AVC decoder. The target application is mobile video, so low power and simplicity are the target design attributes. A prototype of the proposed architecture is implemented in 45 nm CMOS technology. The overall power consumption is 9.01 mW at 140 MHZ. In the second paper, **Full-Hardware Architectures for Data-Dependent Superimposed Training Channel Estimation,** two hardware channel estimator architectures for data-dependent superimposed training (DDST) receiver with perfect synchronization and nonexistent DC-offset are developed. These implementations are demonstration of achieving the required performance for commercial applications. The proposed architectures are prototyped using FPGA and then implemented in 90 nm CMOS technology. The overall power consumption is 3.7 mW and 2.74 mW at 187 MHz and 247 MHz, respectively. The third paper, **VLSI Architecture for MIMO Soft-Input Soft-Output Sphere Detection,** introduces the first soft-input soft-output (SISO) tuple search detector (TSD) hardware implementation. This computational module is scalable in constellation size and number of antennas, it is highly parallel and pipelined. The SISO-TSD architecture is implemented in 65 nmCMOS technology for 4× 4 MIMO transmission and 64-QAM constellation. The prototype has low power consumption of 58.2 mW to 73.9 mW operating at 454 MHz.

The next two papers use FPGA for prototyping and evaluating the proposed algorithms and architectures. The fourth paper, **Multi-source Neural Activity Estimation and Sensor Scheduling: Algorithms and Hardware Implementation,** presents an FPGA prototype of electroencephalography (EEG)/magnetoencephalography (MEG) sensors scheduling algorithm focused on reducing power. The Xilinx Virtex-5 platform shows that it only takes 10 ms to process 100 data

samples using 6400 particles. This performance can support real-time processing of an EEG/MEG neural activity system with sampling rate of up to 10 kHz.

In the fifth paper, **Hardware Acceleration for Neuromorphic Vision Algorithms,** an application specific architecture for accelerating a neuromorphic vision system for object recognition is presented. The architecture is based on HMAX, a biologically-inspired model of the visual cortex. The neuromorphic accelerators are validated on a multi-FPGA system. Results show that the neuromorphic accelerators are 13.8X (2.6X) more power efficient when compared to CPU (GPU) implementation.

The next two papers are examples of prototyping at processor or module level. In the sixth paper, **Integration of Dataflow-based Heterogeneous Multiprocessor Scheduling Techniques in GNU Radio**, a heterogeneous multiprocessor platform is used efficiently to explore design spaces for Software Defined Radio (SDR) system implementation, and examine the overhead of different solutions. In the seventh paper, **Scalable Low-Power Computing via Scheduling on Subsets of Multicore Processors**, presents a novel approach to power management for multi-core processor systems by exploiting the operating system scheduler. Using the various power levels and the utilization statistics of the cores. The execution of software threads is limited to a subset of the available cores while leaving the others idle to allow them to enter into deeper power-saving states. The experimental results show significant thermal power reduction (up to 61 %) in a variety of scenarios, while system performance was sustained in most cases.

The last three papers are using simulation and experimentation for exploring the design space and evaluating the proposed algorithms and architectures. The eighth paper, **A Hardware-Efficient Algorithm for Real-Time Computation of Zadoff-Chu Sequences**, presents a reconfigurable hardware architecture that implement a new algorithm for computing Zadoff-Chu (ZC) sequence elements on-line using the CORDIC algorithm. This architecture is applied in a searcher block for detecting the physical random access channel (PRACH) in Long-Term Evolution (LTE). Simulation tools have been employed for evaluation, results demonstrate that the proposed architecture is capable of achieving detection error rates for LTE PRACH that are close to ideal rates achieved using floating point precision. The ninth paper, **Fast Likelihood Computation in Speech Recognition using Matrices,** explores acoustic modeling using mixtures of multivariate Gaussians. Two case studies are evaluated; direct low-rank approximation of the Gaussian parameter matrix and indirect derivation of low-rank factors of the Gaussian parameter matrix by optimum approximation of the likelihood matrix. Experiments show that both methods lead to similar speedups but the latter leads to far lesser impact on the recognition accuracy. Experiments on 1138 work vocabulary RM1 task and 6224 word vocabulary TIMIT task using Sphinx 3.7 system show that, for a typical case the matrix multiplication based approach leads to overall speedup of 46 % on RM1 task and 115 % for TIMIT task. The final paper, **Soft-Decision Error Correction of NAND Flash Memory with a Turbo Product Code,** presents an error correction scheme for NAND Flash Memory, it is based on The turbo product code (TPC) with multi-precision output. Experimental results, based on a construction rate-0.907 (36116, 32768) extended TPC for 2-bit MLC NAND flash memory, and apply the Chase-Pyndiah decoding algorithm, .are presented for a simulated flash memory channel.

Mohammad Mansour received his B.E. degree with distinction in 1996 and his M.E. degree in 1998 both in computer and communications engineering from the American University of Beirut (AUB), Beirut, Lebanon. In August 2002, Mohammad received his M.S. degree in mathematics from the University of Illinois at Urbana-Champaign (UIUC), Urbana, Illinois, USA. Mohammad also received his Ph.D. in electrical engineering in May 2003 from UIUC. He is currently an Associate Professor of Electrical and Computer Engineering with the ECE department at AUB, Beirut, Lebanon. From December 2006 to August 2008, he was on research leave with QUALCOMM Flarion Technologies in Bridgewater, New Jersey, USA, where he worked on modem design and implementation for 3GPP-LTE, 3GPP2-UMB, and peer-to-peer wireless networking PHY layer standards. From 1998 to 2003, he was a research assistant at the Coordinated Science Laboratory (CSL) at UIUC. During the summer of 2000, he worked at National Semiconductor Corp., San Francisco, CA, with the wireless research group. In 1997 hewas a research assistant at the ECE department at AUB, and in 1996 he was a teaching assistant at the same department. His research interests are VLSI design and implementation for embedded signal processing and wireless communications systems, coding theory and its applications, digital signal processing systems and general purpose computing systems. Prof. Mansour is a member of the Design and Implementation of Signal Processing Systems Technical Committee of the IEEE Signal Processing Society, and a Senior Member of the IEEE. He has been serving as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II since April 2008, Associate Editor for IEEE TRANSACTIONS ON VLSI SYSTEMS since January 2011, and Associate Editor for IEEE SIGNAL PROCESSING LETTERS since January 2012. He served as the Technical Co-Chair of the IEEE Workshop on Signal Processing Systems (SiPS 2011), and as a member of the technical program committee of various international conferences. He

is the recipient of the PHI Kappa PHI Honor Society Award twice in 2000 and 2001, and the recipient of the Hewlett Foundation Fellowship Award in March 2006. He joined the faculty at AUB in October 2003.

Magdy A. Bayoumi received the University of Louisiana at Lafayette 1988 Researcher of the Year Award and the 1993 Distinguished Professor Award. He was an Associate Editor of the IEEE circuits and devices magazine, the IEEE Transactions on Very Large Scale Integration (VLSI) Systems, the IEEE Transactions on Neural Networks, and the IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing. He was an Associate Editor of the Circuits and Devices Magazine and is currently an Associate Editor of Integration, the VLSI Journal, and the Journal of VLSI Signal Processing Systems. He is a Regional Editor for the VLSI Design Journal and on the Advisory Board of the Journal on Microelectronics Systems Integration. From 1991 to 1994, he served on the Distinguished Visitors Program for the IEEE Computer Society, and he is on the Distinguished Lecture Program of the Circuits and Systems Society. He was the Vice President for technical activities of the IEEE Circuits and Systems Society. He was the Cochairman of the Workshop on Computer Architecture for Machine Perception in 1993, and is a Member of the Steering Committee of this workshop. He was the General Chairman of the 1994 MWSCAS and is a Member of the Steering Committee of this symposium. He was the General Chairman for the 8th Great Lake Symposium on VLSI in 1998. He has been on the Technical Program Committee for ISCAS for several years and he was the Publication Chair for ISCAS'99. He was also the General Chairman of the 2000 Workshop on Signal Processing Design and Implementation. He was a founding member of the VLSI Systems and Applications Technical Committee and was its Chairman. He is currently the Chairman of the Technical Committee on Circuits and Systems for Communication and the Technical Committee on Signal Processing Design and Implementation. He is a Member of the Neural Network and the Multimedia Technology Technical Committees. Currently, he is the faculty advisor for the IEEE Computer Student Chapter at the University of Louisiana at Lafayette.

Brian L. Evans is the Engineering Foundation Professor of Electrical and Computer Engineering at The University of Texas at Austin. He earned his BSEECS (1987) degree from the Rose-Hulman Institute of Technology, and his MSEE (1988) and PhDEE (1993) degrees from the Georgia Institute of Technology. From 1993 to 1996, he was a postdoctoral researcher at the University of California, Berkeley. In 1996, he joined the faculty at UT Austin.

Prof. Evans' research bridges the gap between signal processing theory and embedded real-time implementation in the application spaces of digital communications and digital image/video processing. His current research efforts include wireless interference mitigation, powerline communications, smart phone video acquisition and system-level electronic design automation.

Prof. Evans was elevated to Fellow of the IEEE "for contributions to multicarrier communications and image display". In multicarrier communications, his group developed the first linear complexity algorithm that allocates resources to optimize bit rates in multiuser OFDM systems (for cellular and Wimax) and is realizable in fixed-point hardware/software. His group also developed the first ADSL equalizer training method that maximizes a measure of bit rate and is realizable in real-time fixed-point software. In image display, his group's primary contribution is in the design, analysis, and quality assessment of image halftoning by error diffusion for real-time processing by printer pipelines.

Prof. Evans served on the IEEE Design and Implementation of Signal Processing Systems technical committee 1999–2009. The committee guides content, reviews papers and schedules sessions for the entire IEEE Workshop on Signal Processing Systems and for the design and implementation track for the IEEE International Conference on Acoustics, Speech and Signal Processing. He was an Associate Editor for the IEEE Transactions on Image Processing (1998–2002 and 2007–2009) and for the IEEE Transactions on Signal Processing (2005–2009). He has served on the technical program committees for more than 30 IEEE conferences and workshops.

Prof. Evans has published more than 200 refereed conference and journal papers, and graduated 20 PhD and 9 MS students. He has received three teaching awards at UT Austin (2008, 2011 and 2012). He received a 1997 US National Science Foundation CAREER Award.