Guest Editorial

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This issue is devoted to the best work from ASAP 2007, the 18th IEEE International Conference on Application-specific Systems, Architectures and Processors, which was held in Montreal Canada. The ASAP conferences provide a forum for industrial and academic researchers interested in the fundamental principles of applications-specific computing systems and architectures as well as their practical application in a wide variety of domains. The papers selected for revision and extension, which are presented in this issue, reflect this broad role and include solutions to specific application problems such as biological sequence alignment, architectural solutions to problems common in applications specific systems such as communication structures, and explorations of emerging technologies such as quantum dots.

The 7 contributions to this issue were solicited from the authors of the most highly ranked papers in ASAP 2007. These contributions represent significant extensions to the original works and underwent a rigorous refereeing process. We wish to thank the many anonymous referees who contributed to this process for their help in the process of creating and outstanding set of papers.

This issue includes three papers that explore solutions to arithmetic problems. The paper titled “FPGA-Based Efficient Design Approaches for Large

Size Two’s Complement Squarers” by Gao, Chabini, Al-Khalili, and Langlois presents two optimized design approached for two’s complement squarers using embedded multipliers in FPGAs. The first approach is based upon Baugh-Wooley’s algorithm and the second upon a new sign-extension technique which results in substantial improvements in both space and time with respect to traditional methods. The second paper, titled “An Efficient Method for Evaluating Complex Polynomials”, by Ercegovic and Muller, proposes an efficient hardware-oriented method for evaluating complex polynomials which is attractive because of its regular and repetitive structure of simple hardware operators. The third paper, titled “A Novel Cotransformation for LNS Subtraction”, by Vouziz, Collange, and Arnold, gives an overview of the family of Logarithmic Number System (LNS) subtraction algorithms called “Cotransformations” and proposes a novel solution that offers space and time improvements over previous methods without sacrificing accuracy.

Two papers in this issue consist of architectural design explorations implementing specific applications. The paper titled “Design Space Exploration for an ASIP/ Co-Processor Architecture used in GNSS Receivers,” by Kappen, Kurz, Priebe, and Noll, provides an extensive analysis for software/hardware tradeoffs in a platform based upon an attached floating-point coprocessor that can be used for GNSS receivers. The paper titled “Hardware Acceleration of HMMER on FGPAs” by Derrien and Quinton proposes a new hardware parallelization scheme for the hmmsearch function used in biological sequence alignment.

This issue includes one paper exploring communication architectures for complex chip-level systems titled “Design Trade-offs in Customized On-Chip Crossbar

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Schedulers” by Hur, Wong, and Stefanov. The proposed schedulers, which offer significant area improvements over existing solutions, are proposed in order to alleviate scalability issues in conventional crossbar networks.

Finally, we include a “bleeding-edge” paper that explores the application of quantum-dot cellular

automata (QCA) nanotechnology to arithmetic. The paper, titled “Binary Adders on Quantum-Dot Cellular Automata” by Hänninen and Takala describes binary adders with high density and operating frequencies using only a single homogeneous layer of basic cells.

We thank the authors and referees for their contributions to this special issue.