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Introduction to the Special Issue on SAMOS 2007

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This special issue includes a selection of the best papers from the 2007 SAMOS VII Symposium. The International Symposium on Embedded Computer Systems, Architectures, Modeling and Simulation (SAMOS) is an event which annually takes place on the scenic Mediterranean island of Samos. It comprises two co-located events—the International SAMOS Conference and the SAMOS Workshop. In 2007 more than 200 papers were submitted for these two events. After a very competitive selection process only about 30% of these papers have been selected for presentation. According to the Symposium's ranked results and the results of a second stage review process of all presentations from SAMOS, the following eight papers related to architectures and implementations of embedded systems have been selected for publication in this special issue.

We would like to thank all reviewers of the SAMOS Workshop and particularly all reviewers of this special issue for their detailed and intensive review work. The investment of their time and insight is very much appreciated and helped to generate this selection of high quality technical papers.

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The important field of Digital Signal Processor Architectures which is classically one of the focus topics of SAMOS is covered in this special issue by three papers:

Thuresson et al. present a paper which is entitled "FlexCore: Utilizing Exposed Datapath Control for Efficient Computing." Within this paper the authors present a highly efficient DSP architecture and discuss specific elements of this architecture including fine-grained control and a flexible interconnect which lead to significant speedups and significant energy savings. They elaborated on their flexible interconnect that allows the datapath to be dynamically reconfigured as a consequence of code generation. Additionally, the FlexCore provides specialized datapath units to be inserted and utilized within the same architecture and compilation framework.

The problem of memory bottlenecks in modern DSP architectures is addressed by the paper of Pitkaenen et al. which is entitled "Parallel Memory Architecture for Application-Specific Instruction-Set Processors." In this paper, a conflict resolving parallel data memory system for application-specific instruction-set processors is described. The memory structure is generic and reusable to support various application-specific designs. The proposed parallel memory system is attached to an ASIP core and comparisons on area, power, and critical path are presented. Significant power savings can be obtained by exploiting their parallel memory system instead of multi-port memories.

Memory access problems are also addressed in the paper of Galuzzi et al. In "High-bandwidth Address Generation Unit" they present an efficient data fetch circuit to retrieve several operands from an n-way interleaved memory system in a single machine cycle. The proposed address generation unit operates with an improved version of a low-order interleaved memory access approach. The presented design supports data structures of arbitrary lengths and various odd strides.

The second important field of interest which is represented by two papers in this special issue is the field of DSP Frameworks and Optimization Approaches. Ristau et al. introduce "A Mapping Framework Based on Packing for Design Space Exploration of Heterogeneous MPSoCs." The authors show that automating the mapping of applications to a given heterogeneous MPSoC enables not only performance analysis but can also help to refine the system. Therefore, such approaches can be used for design space exploration. The structure of a framework for automatic mapping is presented and it is shown that the mapping problem can be treated as a packing problem which can be solved efficiently by existing optimization software.

In "Applying Data Mapping Techniques to Vector DSPs," Westermann et al. discuss the properties of Vector DSPs. They derive that vector DSPs require input algorithms with vector operations and that the performance of these vectorized algorithms depends to a great extent on the distribution of data with the vector elements. An analysis tool is proposed that focuses on the selection of an efficient dynamic data mapping for vector DSPs.

In the field of Low Power Techniques, the paper "Leakage Aware Multiprocessor Scheduling," authored by de Langen et al., leakage-aware scheduling heuristics are presented that determine the best trade-off between dynamic voltage scaling (DVS), processor shutdown, and finding the optimal number of processors. Experimental results obtained using a public benchmark set of task graphs and real parallel applications show that their approach significantly reduces the total energy consumption compared to an approach that only employs DVS.

The emerging field of Fault Tolerance (FT) is addressed by Borodin et al. in their paper on "Instruction-Level Fault Tolerance Configurability." The authors propose to support instruction-level rather than application-level configurability of FT. This provides a benefit since different parts of some applications (e.g. multimedia) can have different reliability requirements. The paper shows how some existing FT techniques can be adapted to support instruction-level FT configurability, how a programmer can specify the desired FT level of the instructions, and how the compiler can generate these instructions automatically.

The last paper of this special issue stems from the field of Systems and Applications. Yseboodt et al. present "Design of 100 μW Wireless Sensor Nodes on Energy Scavengers for Biomedical Monitoring." This paper focuses on the biomedical area, more specifically on healthcare monitoring applications. Power dissipation is the dominant design constraint in this domain. This paper shows the steps to develop a digital signal processing architecture for a single channel electrocardiogram application, which is used as an application example.

SAMOS 2007 as well as this special issue is dedicated to Prof. Stamatis Vassiliadis, (IEEE Fellow, ACM Fellow, Member of the Dutch Academy of Sciences, and Professor at Delft University of Technology, and two of the guest editors' Ph.D. advisor), who passed away on 7 April, 2007. Born in Manolates, Samos, Stamatis founded the SAMOS conference and workshop series in 2000 and was the heart and soul of the joint events until his death. The series will not be the same without him but it is with great pride we continue in his honor. With this special issue we want to recognize him as an outstanding computer scientist, master inventor, accomplished scholar, and even excellent chef. Because of his vivid and hearty personality he was a good friend to all and particularly to us the editors of this special edition.

The SAMOS series of conferences and workshops will continue as a permanent commemoration to him.

Holger Blume received his Dipl.-Ing. degree in Electrical Engineering from the University of Dortmund, Germany in 1992. From 1993 to 1998 he worked as a research assistant with the Working group on Circuits and Systems for Information Processing of Prof. Dr. H. Schröder in Dortmund. There he finished his Ph.D. on nonlinear fault tolerant interpolation of intermediate images in 1997. In 1998 he joined the Chair of Electrical Engineering and Computer Systems of Prof. Dr. T. G. Noll at the RWTH Aachen University as a senior engineer. There he finished his Habilitation degree on model based exploration of the design space for heterogeneous architectures for

digital video signal processing in February 2008. His main research interests are in the field of design space exploration and heterogeneous reconfigurable Systems on Chip for multimedia applications.

Dr. Blume is chairman of the German chapter of the IEEE Solid State Circuits Society.

Georgi Gaydadjiev was born in Plovdiv, Bulgaria, in 1964. Since 2002 he is assistant professor at the Computer Engineering Laboratory, Delft University of Technology, The Netherlands. His research and development industrial experience includes more than 15 years in hardware and software design at System Engineering Ltd. in Pravetz Bulgaria and Pijnenburg Microelectronics and Software B.V. in Vught, The Netherlands. His research interests include: embedded systems design, advanced computer architectures, hardware/software co-design, VLSI design, cryptographic systems and computer systems testing. Georgi has been a member of many conference program committees at different levels, e.g. ISC, ICS, Computing Frontiers, ICCD, HiPC and more. He was program chair of SAMOS in 2006 and of ICCD in 2008. Georgi received the best paper awards at Usenix/SAGE LISA 2006 and WiSTP 2007. He is HiPEAC, IEEE and ACM member.

Dr. John Glossner is co-founder, CTO, and Executive Vice President at Sandbridge Technologies. Prior to co-founding Sandbridge, John managed both technical and business activities in DSP and Broadband Communications at IBM and Lucent/Starcore. John received a Ph.D. in Computer Architecture from TU Delft in The Netherlands, M.S. degrees in E.E. and Eng. Mgt from NTU, and a B.S.E.E. degree from Penn State. John is a Senior member of the IEEE and has more than 100 publications and 30 issued patents.