Editorial

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In this issue, we have ten articles including two letters. These discuss test and reliability issues of analog circuits, 3D stacked devices, reversible circuits, single event upset, microfluidic devices, memories and adders. One paper deals with hardware security.

The first two papers focus on analog circuits. Dong and Liu of Southwest Petroleum University, Chengdu, China describe their research on fault diagnosis using bispectral analysis. Just as spectrum is the frequency characteristic of a signal, bispectrum combines signal characteristics from two frequencies. One benefit in analog fault diagnosis is that bispectral analysis includes effects of non-linear interactions between frequencies. Bispectral techniques also have clinical applications. In the second paper, Yan, Wang, Liu, Zhou and Long from University of Electronic Science and Technology of China, Chengdu, China use Gaussian noise and Kalman filtering for prognosis of analog circuits. Their objective is to predict the remaining useful life (RUL) of a circuit from the response measured up to the present time.

The third paper addresses testing of through silicon via (TSV) that provides communication among stacks of 3-D devices. Considering the pre-bond testing, Zhang of Apple Inc., Cupertino, CA and Agrawal of Auburn University, Auburn, Alabama, argue that due to differences in contact area the tester probe must connect to multiple TSVs. Their integer linear program minimizes the probing steps, or test time, while maintaining the diagnostic resolution required for repair through available redundant TSVs.

The topic of the fourth paper is reversible circuits. Hasan Babu and Solaiman Mia of University of Dhaka, Bangladesh, and Biswas of University of Texas at Arlington, USA document their research on fault detection and fault correction in reversible circuits. In general, logic circuits have information loss, making them irreversible; lost information becomes unrecoverable as it converts to heat. The idea behind reversible logic is to prevent the loss of information and heat to save energy. An added benefit is the ability to infer the input from output, which leads to fault tolerance. As Michael Frank explains in “*Throwing Computing into Reverse (IEEE Spectrum, September 2017, pp. 32-37)*,” reversible computing is not there yet but is coming soon, making it highly relevant for research.

The fifth paper provides a method for hardening a circuit against single event upset (SEU). Authors are Hamad and Savaria of Polytechnique Montreal, Montreal, Canada, and Mohamed of Concordia University, Montreal, Canada. After identifying parts of the circuit with high vulnerability to SEU, they resynthesize those parts for enhanced logical and temporal masking of errors.

The sixth paper offers test procedures for the micro-electrode-dot-array (MEDA) architecture of fluidic devices. These devices have biomedical applications. Although the operation here is digital, an oscillation-based testing (OBT) is used. Contributors are Shukla, Hussin and Hamid from Universiti Teknologi Petronas, Malaysia, Ali from Waham Technologies, Subhang Jaya, Selangor Darul Ehsan, Malaysia, and Chakrabarty from Duke University, Durham, NC, USA. This is a novel application of OBT, originally proposed about two decades ago by K. Arabi and B. Kaminska for testing of analog circuits. For readers new to the subject, G. H. Sánchez, et al. report several applications of OBT in a book, *Oscillation-Based Test in Mixed-Signal Circuits* (Springer, 2006).

Next, the seventh paper exposes an aging related failure mechanism of a static random access memory (SRAM).

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Authors point out that some resistive defects, which escape the manufacturing test, can accelerate the age-related failures caused by negative-bias temperature instability (NBTI). The paper analyzes this phenomenon and attempts to quantify the loss of reliability. Contributors of this work are Martins, Medeiros, Copetti, Vargas, and Bolzani Poehls of Pontifical Catholic University of Rio Grande do Sul (PUCRS), Porto Alegre, Brazil.

The eighth contribution addresses a problem in hardware security. As a chip design goes through manufacturing stages, its function may be interpreted from the physical design for malicious purposes. This paper presents low overhead designs of threshold voltage defined (TVD) logic gates. In TVD gates, a common physical structure is used for various Boolean functions such that any specific functions can be achieved by controlling threshold voltages of transistors during processing. Thus, the function of the circuit is not interpretable from the

physical layout alone. The authors are Rathor, Garg and Sharma of ABV- Indian Institute of Information Technology and Management, Gwalior, India.

In the first *JETTA Letter*, Jung and Sung of Samsung Electronics Company, Hwaseong-si, South Korea, and Choi of Sungkyunkwan University, Suwon-si, South Korea present a new technique for measuring the sensitivity of threshold voltage with respect to the body bias voltage in a dynamic random access memory (DRAM). The second *letter*, by Geetha and Amritvalli from Coimbatore Institute of Technology, Coimbatore, India, gives a design for an adder circuit with a compromise in the accuracy of lower order bits to levels acceptable for specific applications while reducing the delay and gate count.

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Editor-in-Chief