Editorial

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I am pleased to announce the *2015 JETTA-TTTC Best Paper Award*. The award committee of the Test Technology Technical Council (TTTC) once again consisted of Matteo Sonza Reorda (Chair), Vishwani Agrawal, Salvador Mir, Adit Singh and Xiaoqing Wen. We congratulate the winning authors, Nicholas Tzou, Debesh Bhatta, Barry J. Muldrey Jr., Thomas Moon, Xian Wang, Hyun Choi and Abhijit Chatterjee. Their paper, “Low Cost Sparse Multiband Signal Characterization Using Asynchronous Multi-Rate Sampling: Algorithms and Hardware,” appeared in the *Journal of Electronic Testing: Theory and Applications*, Volume 31, Number 1, pp. 85–98, February 2015. The research reported in the paper was performed at the Georgia Institute of Technology, Atlanta, Georgia, USA. See the award announcement pages in this issue.

Closing the year 2016 and completing thirty-second volume of *JETTA*, this issue contains seven papers and one letter. The topics discussed are analog and RF circuit modeling, test and diagnosis, reliability assessment, test compaction, and FPGA testing.

The first paper defines a new format for fault dictionary of an analog circuit and then using an entropy measure selects a minimal set of test point to enhance fault diagnosis. Authors are Cui, Shi and Wang from Beihang University, Beijing, China.

The second paper focuses on early detection of anomalous behavior (performance parameters being out of the specification range) of an analog filter, which may also provide an

assessment of the residual useful life (RUL) of the device. The authors use statistical concepts of Mahalanobis distance (MD) and Parzen window. The paper is contributed by Hu, Xiao, Zhang, Liu and Ge from Air Force Engineering University, Baqiao, Shanxi Xi’an, China.

The third paper examines processor errors caused by single event upsets (SEU) in the instruction memory. Determination of the mean time to failure (MTTF) shows that unless certain conditions are satisfied, protection of the memory by error correcting codes (ECC) and scrubbing (checking and writing back) may not be effective. This research is reported by Q. Chen, L. Chen, Wang, Wu, Li, Zhao and M. Chen from Xi’an Microelectronics Technology Institute, Xi’an, Shaanxi, China, University of Saskatchewan, Saskatoon, SK, Canada, Hohai University, Jiangsu, China, and Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China.

The fourth paper employs a breadth-first data mining algorithm to extract assertions from simulation data. Matching of assertions with specifications then formally verifies the correctness of the simulated hardware. This research is reported by Hanafy of Mentor Graphics in Cairo, Egypt, and Said and Wahba from Ain Shams University, Cairo, Egypt. Parts of this work were reported at the 24th *IEEE North Atlantic Test Workshop*, Johnson City, NY, USA, May 11–13, 2015. The paper appearing here is an enhanced version that authors prepared for *JETTA*. We thank Dr. Krishna Chakravadhanula, Guest Editor, for conducting the peer review process for the journal version.

The fifth paper provides a method for timing characterization of an intellectual property (IP) library used in the design of system-on-chip (SoC) devices. As an example, process-voltage-temperature (PVT) effects in a 28 nm fully depleted silicon on insulator (FD-SOI) technology library are examined. Contributors are Juneja, Immadi, Singh and Agarwal from STMicroelectronics, Greater Noida, India, Patel and

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Naudet from STMicroelectronics, Crolles, France, and Virazel and Girard from LIRMM, France.

Test compaction is a serious concern in the industry today, caused by the enormous test data required for complex VLSI devices. Addressing this topic, the sixth paper presents an optimal selective count compatible run length (OSCCPRL) encoding scheme that demonstrates 80 % test compression efficiency. Authors are Vohra from Thaper University, Patiala, Punjab, India, Singh from Punjabi University, Patiala, Punjab, India, and SenGupta from Indian Institute of Technology, Kharagpur, West Bengal, India.

The seventh paper gives a generic procedure for testing both global and local interconnects of an FPGA. Although an example of Xilinx Virtex Series is used the paper claims

that the method is applicable to FPGAs of any type or size. Authors are Ruan, Huang, Wang and Zhao from University of Electronic Science and Technology of China, Chengdu, China.

We end the issue with a *Letter* by Jun, Ping and Kai from Hangzhou Dianzi University, Hangzhou, China. They present an S-parameter model extraction method for partially depleted silicon on insulator metal oxide semiconductor field effect transistor (PD SOI MOSFET). They show excellent agreement between the measured and simulated output admittances of a manufactured device.

At the time this issue goes to press, *JETTA* Editorial Board annual meeting is scheduled for Fort Worth, Texas on November 16, 2016.