Editorial

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Received: 3 September 2016 / Accepted: 3 September 2016 / Published online: 9 September 2016
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This issue contains eight papers and two *Letters*. These articles focus on testing of three-dimensional stacked devices, analog circuits and delay faults. In addition, reliability, fault tolerance and security aspects are addressed. We also have one paper on accelerating the test pattern generation program by using multiprocessing. The two letters discuss test compression and compact modeling of inductors at radio frequency, respectively.

The first paper gives the design of an IEEE-1500 conformant test wrapper for a core in a 3D-stacked system-on-chip (SoC). Specifically, when a core is distributed among layers the proposed design minimizes the number of through silicon via (TSV) used by the wrapper. Authors are Roy, Giri and Rahaman from Indian Institute of Engineering Science and Technology, Shibpur, Howrah, West Bengal, India.

Next, a paper on analog circuit fault diagnosis focuses on parametric faults. The authors employ several machine learning methods to improve the diagnosis precision to levels generally associated with catastrophic faults. The paper is contributed by Zhang, Y. He, Yuan, W. He, Xiang and Li from Hefei University of Technology, Hefei, China.

Reliability and fault tolerance are discussed in the next three papers. First, a paper demonstrates how the operational reliability of an interconnection bus of a multiprocessing system can be assessed. A newly introduced parameter *BloRel* characterizes the operation of the network under various scenarios. This paper is authored by Bistouni and Jahanshahi of Islamic Azad University, Tehran, Iran.

The second paper in the fault tolerance group addresses the soft error effects in asynchronous circuitry implemented in submicron technologies. Authors take an unconventional approach of modeling the circuit behavior and potential soft errors using linear temporal logic (LTL), which is then analyzed by a formal model checker. Contributors are Lodhi and O. Hasan from National University of Sciences and Technology (NUST), Islamabad, Pakistan, S. R. Hasan from Tennessee Technological University, Cookeville, TN, USA, and Awwad from United Arab Emirates University, Al-Ain, UAE.

The third paper in the fault tolerance group is authored by Nandha Kumar and Almurib from The University of Nottingham, Malaysia, Semenyih, Malaysia, and Lombardi from Northeastern University, Boston, MA, USA. They examine the reliability of a static random access memory (SRAM) implemented with memristers. Such memories are useful as look up tables (LUT) of an FPGA due to small area, high speed and low power, but their reliability degrades with time as switching cycles increase. The paper establishes a relationship between memristor deterioration and current, the latter being an easily observable parameter.

The next paper is on delay testing and is authored by Shintani, Uezono and Sato of Kyoto University, Kyoto, Japan, Hatayama of Gunma University, Gunma, Japan, and Masu of Tokyo Institute of Technology, Yokohama, Japan. By using a path clustering technique the authors show up to 90 % reduction in the number of delay tests without compromising on parametric fault coverage (PFC). The PFC is computed through Monte Carlo simulation considering random variations of threshold voltages.

Hardware security is addressed in the seventh paper of this issue, contributed by Dofe, Pahlevanzadeh and Yu from University of New Hampshire, Durham, NH, USA. The

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authors focus on countermeasures for preventing malicious attempts to retrieve the secret key of a cryptosystem. Their work examines the effectiveness of countermeasures when multiple attack mechanisms are used.

In the eighth paper, the authors use multiprocessing to speed up automatic test pattern generation (ATPG). As usual, faults are distributed on processors. However, the work of processors is coordinated through a procedure called circular pipeline processing (CPP). This leads to patterns that are deterministic and hence the ATPG is repeatable. This research is reported by Yeh and Huang of National Taiwan University, Taipei, Taiwan, and Wang from SynTest Technologies, Inc., Sunnyvale, CA, USA.

In the first *Letter*, Yuan, Ju, Guo and Wang from Beijing University of Technology, Beijing, China, and Sun from Tsinghua University, Beijing, China, discuss a test data encoding method for higher compression ratio and shorter test application time. They also give a simple and compact decoder.

The second *Letter*, contributed by Hou and Wang from Beijing University of Posts and Telecommunications, Beijing, China, T. Liu and Yu from Zhejiang University, Hangzhou, China, J. Liu from Hangzhou Dianzi University, Hangzhou, China, and Chen from Shanghai Jiao Tong University, Shanghai, China, presents a compact model of an inductor for use in design and simulation of radio frequency systems.