Editorial

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This issue contains eight papers and two *Letters*. The topics discussed in these articles are 3D-stacked IC test, design verification and debug, fault tolerance and reliability, test of reversible logic, reduced pin-count test, testing of power regulators, and design and test of an RF power amplifier. The second, sixth and eighth papers are derived from the program of the *Sixteenth IEEE Latin American Test Symposium (LATS)*, Puerto Vallarta, Mexico, March 25–27, 2015. Guest Editor Leticia Maria Bolzani Poehls deserves credit for editing these papers.

The first paper describes the design of a built-in self-test system for a 3D stacked memory device. It tests the memory, interface circuitry and through silicon vias (TSV). Ideas and design are contributed by Luo, Wu, Hsu and Chen from Industrial Technology Research Institute, Hsinchu, Taiwan, ROC.

In the second paper, Poulos and Veneris from University of Toronto, Toronto, Ontario, Canada discuss debugging. Their method involves first classifying faults into categories and then clustering them based on similarity.

Fault tolerance and reliability is the theme for the next three papers. The first paper in this group provides a static memory cell hardened against single event upset (SEU). The new design adds four transistors to a six-transistor SRAM cell. Authors are Y. Li, L. Chen, Liu, Wang, Newton and M. Chen from University of Saskatchewan, Saskatoon, SK, Canada, L. Li and Ma from Dalhousie University, Halifax,

NS, Canada, and Wu from China University of Petroleum, Qingdao, China.

The second paper in the fault tolerance group provides protection against SEU in a pipeline processor by inserting redundancy in the combinational logic. Contributors are Wali, Virazel, Bosio, Girard and Pravossoudovitch from University of Montpellier/CNRS, Montpellier, France, and Sonza Reorda from Politecnico di Torino, Torino, Italy.

Continuing with the theme of fault tolerance the third paper in the group employs the finite element method to simulate how noise sources affect an integrated circuit. The sources considered are device noise (thermal, shot and flicker), switching noise due to logic activity, and SEU. Authors of this paper are Melo and Torres of Universidade Federal de Minas Gerais, Belo Horizonte, MG, Brazil.

Next two papers discuss theoretical developments. The first of these is authored by Nagamani, Ashwin, Abhishek and Agrawal from PES Institute of Technology, Bangalore, Karnataka, India. They derive algorithms for testing single and multiple stuck-at faults, repeated gate faults, and missing gate faults in reversible logic circuits. The second paper is contributed by Can, Kassim and Fischer from Friedrich-Alexander-University Erlangen-Nuremberg FAU, Erlangen, Germany. Their ternary-vector-list format results in compact representation of Boolean functions and efficient test generation.

The eighth paper introduces a multi-valued logic interface between automatic test equipment (ATE) and a digital device under test (DUT). The method, involving analog signal transmission through mixed-signal data converters, facilitates reduced pin-count test. The work is reported by Li and Agrawal from Auburn University, Auburn, Alabama, USA.

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The first of two *JETTA Letters* is contributed by Nguyen, Ozmen, Dirican, Tan and Margala from University of Massachusetts Lowell, Lowell, MA, USA. Their built-in sensor for checking the reliability of a power supply regulator can detect output ripples as

small as 50 mV. In the second *letter* Lin, Cheng, Gu, Zhu and Fu from Tianjin University, Tianjin, China, and Chen from Qinghai University for Nationalities, Qinghai, China discuss design and test of a broadband radio frequency power amplifier.