Editorial

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We begin 2016 with five additions to the editorial board of *JETTA*. New editors are Enamul Amyeen, Swarup Bhunia, Leticia Maria Bolzani Poehls, Suraj Sindia and Mehdi Tahoori. Their pictures and biographies appear in this issue.

Retiring from the board are Bashir M. Al-Hashimi, Melvin A. Breuer and Joan Figueras. Each has served the journal for several years and we gratefully acknowledge their contributions.

Peer reviews are essential for maintaining the standard of *JETTA*. We thank our reviewers for contributing their expertise and time. A list of those who completed reviews for *JETTA* in 2015 appears in this issue.

This issue contains seven papers and one *Letter*. The topics discussed in these articles are single event upset, test scheduling, fault tolerance, and diagnosis of analog circuits. The second, fourth and sixth papers are derived from the program of the *Sixteenth IEEE Latin American Test Symposium (LATS)*, Puerto Vallarta, Mexico, March 25–27, 2015. Guest Editor Leticia Maria Bolzani Poehls deserves credit for editing these papers. I am happy to observe that starting this year she will join our editorial board as a regular editor.

To begin, we have two papers discussing the single event upset (SEU) phenomenon. First, Y. Li, Wang, L. Chen, Liu and M. Chen from University of Saskatchewan, Saskatoon, SK, Canada and L. Li from Dalhousie University, Halifax, NS, Canada, present the design of an SEU detector circuit. Their implementation in 65 nm technology using dual modular redundancy for error correction requires reduced area and power over conventional triple modular redundancy circuits.

The next paper provides a design of a ring oscillator whose frequency drift indicates strikes by ionized particles. Authors, Coulié-Castellani, Rahajandraibe, Aziza and Portal from Université de Toulon, Marseille, France, and Micolau from Université d'Avignon, Avignon, France, emphasize enhanced particle detection sensitivity over previous designs.

The third paper addresses test time minimization for a system-on-chip that contains programmable interconnection network. The network is modeled as a graph to analyze paths for test access and an evolutionary algorithm then finds an optimal schedule for core tests that must conform to given power constraints. The reported research is contributed by Hu and Li from Xidian University, Xi'an, China, and Xu and Jia from Guilin University of Electronic Technology, Guilin, China.

In the fourth paper, Ferraretto and Pravadelli from University of Verona, Verona, Italy, evaluate dependability of embedded systems in the presence of hardware faults. They use an instruction-level architectural emulator named QEMU that is capable of injecting both permanent and intermittent faults.

Test data compression is the theme of the fifth paper authored by Yuan, Guo and Ju from Beijing University of Technology, Beijing, China, and Sun from Tsinghua University, Beijing, China. Their technique combines test reordering, don't care filling and a power efficient alternating statistical run-length (ASRL) encoding. Such methods are useful in today's testing practice where large test data volume, high power consumption and long test time are serious considerations.

Next, we have two papers on analog circuit test. Azaïs, David-Grignot and Latorre from LIRMM, Université Montpellier, France, and Lefevre from NXP Semiconductors, Caen, France, propose the use of fast Fourier transform (FFT) for measuring phase noise of an analog circuit on a digital tester.

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Tang and Xu from Naval Aeronautical and Astronautical University, Jinan, Shandong, China, propose a diagnosis methodology. They analyze the response of a circuit under test to identify measurable quantities (features) whose determination will minimize the ambiguity in distinguishing between pairs of faults. Ambiguity is mathematically defined and is computable from probability density functions of the feature with respect to random variations of circuit component values.

A *JETTA Letter* is contributed by Wang and Dai from Hohai University, Changzhou, China, Li and Chen from

University of Saskatchewan, Saskatoon, SK, Canada, and Shi and Guo from China Institute of Atomic Energy, Beijing, China. They argue that radiation hardening of dynamic logic must differ from that of static circuits. Their design proposal claims lower area and power overheads.

Appearing at the end is a correction to a recent paper, “Speeding up Logic Locking via Fault Emulation and Dynamic Multiple Fault Injection,” by Gören, Gürsoy and Yildiz, published in *JETTA*, volume 31, number 5/6, pp. 525–536, December 2015.