Editorial

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To begin this double issue of October and December 2015, I am pleased to announce the *2014 JETTA-TTTC Best Paper Award*. The award committee appointed by the Test Technology Technical Council (TTTC) Chair, Michael Nicolaidis, was the same as in 2013 and consisted of Matteo Sonza Reorda (Chair), Vishwani Agrawal, Salvador Mir, Adit Singh and Xiaoqing Wen. We congratulate the winning authors, Rafal Baranowski, Michael A. Kochte and Hans-Joachim Wunderlich. Their paper, “Access Port Protection for Reconfigurable Scan Networks,” appeared in *JETTA*, Volume 30, Number 6, pages 711–723, December 2014. The photograph here shows Hans-Joachim Wunderlich (left) receiving the award from the TTTC President, Yervant Zorian, at the International Test Conference in Anaheim, California, on October 8, 2015. See the award page in this issue.

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This joint October-December issue of *JETTA* contains nine papers and one letter. The topics discussed are VLSI yield, analog and radio frequency circuit testing, 3D stacked integrated circuit testing, hardware security, soft error tolerance and automatic test equipment (ATE) technology.

The first paper discusses a yield enhancement methodology. Authors, Hsieh, Wang, Kuo, Huang and Chih of National Sun Yat-sen University, Kaohsiung, Taiwan, pursue the idea that certain faults that merely degrade performance leaving the function otherwise intact can be tolerated in the sense of producing usable devices.

The next four papers focus on analog and RF circuit testing. The first of these provides digital testing methods for measuring phase noise or jitter. Depending upon the available oversampling rate as many as 32 devices can be tested in parallel. Authors are David-Grignot, Azaïs and Latorre of Université Montpellier, France and Lefevre from NXP Semiconductors in France.

The next paper in the analog and RF group explores the possibility that the occurrence of a fault may not cause an instant failure but in fact reduce the remaining useful life (RUL) of the circuit. The new test methodology attempts to predict the impending failures as circuit components degrade. This research is contributed by Hu, Xiao, Zhang, Song and Yang from Air Force Engineering University in Shanxi Xi'an, China.

The third analog and RF paper addresses minimization of specification tests by preserving the defect level. The method relies on Monte Carlo simulation and integer linear programming. Given that test time and cost are serious considerations, demonstration of 50 % reduction seems significant. Authors are Sindia of Intel Corporation, Hillsboro, Oregon and Agrawal of Auburn University in Alabama. An earlier version of this work was presented at the 15th IEEE Latin American Test Workshop, Fortaleza, Brazil, 12–15 March, 2014 and the review process of the present version for *JETTA* was conducted by Leticia M. Bolzani Pöhls as Guest Editor.

The fourth paper on analog circuit test gives a dictionary based diagnosis method for nonlinear circuits. Contributors are Tadeusiewicz, Kuczyński and Hałas from Lodz University of Technology, Łódź, Poland.

Next, we have a paper on 3D stacked integrated circuits authored by Aghaee, Peng and Eles from Linköping University in Sweden. They rearrange tests to cause accelerated temperature cycling during test. Thus, many early life failures can be isolated without the need for expensive life testing.

Hardware security is discussed in a paper by Gören, Gürsoy and Yildiz of Yeditepe University, Istanbul, Turkey. The authors use FPGA based fault emulation to determine sites for fault injection elements (FIE) in a circuit with logic locking. Such a design would function correctly only when a specified key input is applied to deactivate FIEs.

Authors Li, Wang, Yao, Yan, Gao and Xu, working at University of Saskatchewan, Saskatoon, Canada, Hohai University, Changzhou, China and Tianjin University, Tianjin, China, present their radiation hardened design of a latch in the next paper. Both space and time redundancies are combined to suppress soft errors. An implementation in 180 nm technology demonstrates reduced performance penalty compared to other similar designs.

Providing timing accuracy in digital test waveform, an important function of the automatic test equipment (ATE), is the focus of the next paper. Chen, J-L Huang, Kuo and X-L Huang from National Taiwan University, Taipei, Taiwan, OpenATE Incorporated, Taipei, Taiwan and Industrial Technology Research Institute, Zhudong, Hsinchu, Taiwan, achieve a 20 ps timing resolution from their FPGA based design of a timing formatter.

We end this issue with a *Letter* by Li and Ma from Dalhousie University, Halifax, Canada, Li, Wang, Liu, Newton and Chen from University of Saskatchewan, Saskatoon, Canada, and Wu from China University of Petroleum, Qingdao, China. Their layout of a six-transistor SRAM cell has higher tolerance against single event upsets.

JETTA Editorial Board held its annual meeting at Anaheim, California on October 7, 2015. This photograph taken at the meeting shows (left to right) editors Vishwani Agrawal, Krishnendu Chakrabarty, Andre Ivanov, Sybille Hellebrand, Mark Tehranipoor, Erik Jan. Marinissen, Tian Xia, Hans-Joachim Wunderlich, Shawn Blanton, Adit Singh, Yiorgos Makris, Haralampos Stratigopoulos and Stephen Sunter, and Charles Glaser, Executive Editor, Springer.