Editorial

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This issue contains eight papers and two letters. Topics covered are simulation, verification, radiation effects and single event upsets, microprocessor test, power constrained testing, and analog circuit testing. The fourth and eighth papers originated from presentations at the 2013 Latin American Test Workshop, Cordoba, Argentina. We are thankful to guest editor, Raoul Velazco, for the processing of one of these papers.

The first paper surveys Verilog simulation systems using a variety of techniques ranging from multiprocessing to hardware assisted methods, outlining capabilities, limitations and possible future directions. Authors are Tan of Altera Corporation, Penang, Malaysia and Affendi bin Rosdi from Universiti Sains Malaysia, Penang, Malaysia.

The second paper contributes to the area of compact modeling of interconnects. To allow scalability in the simulation of large VLSI devices a partitioning method is proposed such that the model order reduction is applied to partitions rather than to the whole. This contribution comes from Miettinen, Honkala and Valtonen from Aalto University School of Electrical Engineering, Aalto, Finland and Roos of AWR-APLAC Corporation, Espoo, Finland.

The third paper is about formal verification. Its novelty is in decomposing complex properties into simpler sub-properties for which tests are easier to generate. Authors are Chen from East China Normal University, Shanghai, China, and Qin and Mishra from University of Florida, Gainesville, Florida, USA.

In the fourth paper soft errors in graphics processing units (GPUs) are discussed by Rech and Carro from Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil, and Frost

of Rutherford Appleton Laboratories, Didcot, UK. A notable finding from their radiation experiment is that floating point computations are relatively more reliable than integer operations.

Microprocessor test is featured in the fifth paper by de Carvalho, Bernardi, Sanchez and Sonza Reorda from Politecnico di Torino, Italy and Ballan of STMicroelectronics, Italy. To increase the coverage of functionally testable faults they insert test hardware. This hardware assists in setting signal states necessary for detecting faults that are otherwise hard to test.

In the sixth paper, Arvaniti and Tsiatouhas from University of Ioannina, Ioannina, Greece, address the problem of excessive power consumption during the scan operation of test. Their method of partitioning the scan registers such that partitions can be independently bypassed allows them to reduce the circuit activity to any desired level.

Next, we note that the test of an analog circuit contains more than just the pass-fail information. Test data can be analyzed to determine the state of hardware degradation (aging) or, more specifically, to decide how long a passing system is likely to go on before it fails. To find out how this might be done, see the paper by Zhang from Normal University, China and He, Yuan and Deng from Hefei University of Technology, China.

The Nobel Prize in Physics for 2010 was awarded to Andre Geim and Konstantin Novoselov of University of Manchester “for groundbreaking experiments regarding the two-dimensional material graphene.” Made of pure carbon, graphene has a hexagonal honeycomb structure of atoms and possesses physical and electrical properties that resemble no other material we have known before. Many applications are being found, one of which is a new transistor discussed in the next paper by Oleiro and Bolzani Pöhls from Catholic University of Rio Grande do Sul, Porto Alegre, Brazil, and Miryala, Calimera,

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Macii and Poncino from Politecnico di Torino, Torino, Italy. Their focus is on modeling of faults.

The first of the two Letters is authored by Wang and Li from South West Agriculture University, Chongqing, China, and Chen and Meng of China University of Geosciences,

Wuhan, China. They propose a genetic algorithm for selecting test points to improve testability.

The second Letter is authored by Ren and Chen of University of Saskatchewan, Saskatoon, Canada. They study the effects of single event transients in analog and mixed-signal circuits.