Editorial

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The term “DFT” has several meanings. If you work in testing then DFT is “design for testability.” For signal processing folks it means “discrete Fourier transform.” In recent years, submicron VLSI and nanotechnology have given a new meaning to DFT, *defect and fault tolerance*. As device sizes shrink to nanometer dimensions, several phenomena begin to affect the operation. Single event upsets (SEU) were known to hamper the proper function of large memories, especially at high altitudes. Now SEU have become relevant to logic, in addition to memory, and at the ground level, in addition to the high altitude. Nanometer dimensions are so small that control mechanisms used in various types of processes, namely, chemical, mechanical and optical, used in VLSI manufacturing have to be reinvented. The present state of the art demands that we allow larger random variations in dimensions of transistors and interconnects on chips. To guarantee correct electrical behavior we must design systems knowing that its components will be affected by permanent defects due to process variation and transient errors due to SEU. That gives us an opportunity to use the known techniques for fault tolerance and invent new ones when necessary.

The DFT 2013 or *15th IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, to be held in New York during October 2–4, 2013, has a 25 year history. It started as an annual workshop named DFT 1988. After 10 years, the DFT 1998, i.e., the eleventh workshop was elevated to a symposium level and renamed as the First DFT Symposium.

JETTA has devoted several special issues to this timely topic. Two recent ones were published in February 2008 (volume 24, numbers 1, 2 and 3, Guest Editors – Nur Touba, Adelio Salsano and Minsu Choi, 25 papers) and February 2009 (volume 25, number 1, Guest Editors – Cristiana Bolchini and Yong-Bin Kim, 9 papers).

We are now pleased to bring out this special issue of *JETTA* based on the DFT 2011, *14th IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*. I must thank Guest Editors, Prashant Joshi and Massimo Violante, for their contributions in putting it together. There are 13 papers appearing here and a few more will follow in the next issue. Please read their guest editorial for a summary of this issue.

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