Guest Editorial

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The IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS) is an annual event providing an open forum for presentations in the field of defect and fault tolerance in VLSI systems. All aspects of design, manufacturing, test, reliability, and availability that are affected by defects during manufacturing and by faults during system operation are of interest. In recent years, new technologies such as Carbon Nanotube Field-Effect Transistor appeared and, recognizing their relevance, DFTS evolved its scope that today embraces both VLSI and nanotechnology.

This Special Issue collects the best papers from the 2011 edition of DFTS, which took place in Vancouver, British Columbia, and covers the full spectrum of topics of DFTS.

The section *Defects, faults, and test techniques* opens with faults affecting nanotechnologies with a paper by Lombardi et al. focused on the delay of a CNTFET with undeposited CNTs by gate width adjustment; the following paper by Dworak et al. covers the aspect of test optimization presenting a simulated annealing inspired test optimization method for enhanced detection of highly critical faults and defects; the last paper of this section by Teixeira et al. focuses on process variation-aware statistical analysis framework for aging sensors insertion.

In recognition of the growing relevance of soft errors, the next section of this special issue is entitled *Transient event effects and fault tolerant design*. The section opens with a

paper by Costenaro et al. entitled a practical approach to single event transient analysis for highly complex design, followed by a paper by Gangadhar et al. that deals with a probabilistic approach to diagnose single event transients in sequential circuits, and another paper by Bastos et al. proposing a new recovery scheme against short-to-long duration transient faults in combinational logic. The section closes with a paper by Alderighi et al. who discuss a preliminary study about SEU effects on programmable interconnections of SRAM-based FPGAs.

As the nature of DFTS is both fault/defect modeling and testing and fault tolerance, the special issue also contains two sections devoted to fault tolerant design techniques. The section entitled *Analysis of faults and fault tolerant design for microprocessors and memories* opens with Karimi et al. discussing the impact of performance faults in modern microprocessors; and continues with Soucarros et al. reporting a fault analysis and evaluation of true random number generators embedded in a processor. Next two papers focus on error correction: Bonnoit et al. discuss the use of error correcting codes without speed penalty in embedded memories: algorithm, implementation and case study, while Omana et al. present a low cost concurrent error detection strategy for the control logic of high performance microprocessors and its application to the instruction decoder.

The last section focuses the attention on *Fault tolerant network-on-chip design*. Fukushima et al. discuss a region-based fault-tolerant routing algorithm for 2D irregular mesh network-on-chip, and Latif et al. discuss partial virtual channel sharing: a generic methodology to enhance resource management and fault tolerance in networks-on-chip.

As the number of papers selected from DFTS 2011 was rather large for a single issue, remaining papers will appear in the next issue of JETTA. We hope you will find this

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special issue exciting. We would like to close this guest editorial by recognizing the efforts and the patience of all authors and the reviewers who contributed to this special issue.

Prashant D. Joshi received his B.Tech. degree from IIT Bombay and his MS from the University of South Carolina, both in Computer Science. Prashant works with Intel Corporation. His design experience encompasses all phases of microprocessor design from custom circuits, cell based design, performance validation, noise analysis, pre-Si validation, etc., on chips ranging from the Intel® 486, Intel® Pentium II™, Intel® Pentium 4™ and their derivatives all the way to Intel® Atom™ processors. He has also worked with IBM and Broadcom in the past. His areas of interest are in the design of cutting edge microprocessors, graph theory and reliability. Prashant has published about 15 papers and

holds a patent. He has been involved with several conferences and workshops in the past. Recently, he served on the IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems as a program co-chair in 2011 and as general co-chair in 2012.

Massimo Violante received the MS and PhD degrees from Politecnico di Torino, Italy, where he is now an Associate Professor. Prof. Violante's main research topic is the design and validation of embedded system for safety and mission critical applications, with particular emphasis on the use of commercial off-the-shelf components like processors and Field Programmable Gate Arrays. Prof. Violante has published more than 150 papers in the area of testing and designing reliable embedded systems and he has co-authored two books. He served as a program co-chair of the IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems in 2011 and as program chair of the IEEE European Test Symposium in 2012.