Editorial

Vishwani D. Agrawal

Received: 24 March 2013 / Accepted: 24 March 2013 / Published online: 6 April 2013
© Springer Science+Business Media New York 2013

This is a special issue based on the *First Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale* (MEDIAN 2012), Annecy, France, held on June 1, 2012. The plan for a special issue was announced at the workshop. Four papers selected from the submitted set of papers appear here. I am thankful to Guest Editors, Dimitris Gizopoulos, Said Hamdioui and Hans Manhaeve for carrying out the journal's peer review process. They introduce the papers in a guest editorial that follows the TTTC Newsletter. The second workshop in this series, MEDIAN 2013, will be held in Avignon, France, May 30-31, 2013. You can find out more from <http://www.median-project.eu/median2013.htm>.

Following the four special issue papers, this issue contains regularly submitted four papers and three *Letters*. The third and fourth papers were selected from the program of the *IEEE Latin-American Test Workshop* (LATW) of 2012 through the journal's review process. The topics covered are concurrent error detection, security, dependable embedded systems, verification, analog circuit test, scan architecture and single event transient detection sensor.

The first of the regular papers is contributed by Kehl of Bosch Engineering GmbH, Abstatt, Germany, and Rosenstiel of University of Tübingen, Tübingen, Germany. They use redundancy in the state assignment for online error detection in a finite state machine. The proposed redundancy scheme is less restrictive than those used before and results in lower overheads.

The authors of the next paper are Das, Ghosh, Seys and Verbauwhede from Leuven, Belgium, and Da Rolt, Dupuis, Di Natale, Flottes and Rouzeyre from LIRMM, Montpellier, France. They provide secure communication between a tester and a system under test using provably secure asymmetric key

based authentication and verification protocols built into the JTAG interface.

The next paper is authored by Bergaoui, Wecxsteen and Leveugle of TIMA Laboratory, France. They find that a compiler optimization of a program can increase the sensitivity of a computing system to soft errors. The lifetime of a program variable in a storage device, memory or register file, determines its sensitivity to soft error. The investigation concludes that the choice of optimization options at compile time can have a strong impact on the dependability of the computation.

The fourth regular paper is authored by Romero, Strum and Chau of University of Sao Paulo, Sao Paulo, Brazil. They describe experiments on coverage driven verification using two circuits with large and small input spaces, respectively.

In the first *JETTA Letter*, Kavithamani and Manikandan from Coimbatore Institute of Technology, Coimbatore, India, and Devarajan from Government College of Technology, Coimbatore, India, use neural networks to identify component faults of an analog circuit from input current, output voltage and output current that are easily measured without accessing the internal nodes of the circuit.

The second *letter* is authored by Chakraborty of Lattice Semiconductor, Hillsboro, Oregon, USA, and Kelly and Evans of Camgian Microsystems, Starkville, Mississippi, USA. They propose a new scan structure that avoids the problems related to power supply noise and hold time.

The final contribution of this issue is a *letter* by Zhang, Ren, Chen and Sammynaiken from University of Saskatchewan, Saskatoon, Saskatchewan, Canada, Gaspard, Witulski, Holman and Bhuvra from Vanderbilt University, Nashville, Tennessee, USA, and Wen from Cisco Inc., San Jose, California, USA. They design an eight-transistor voltage sensor to detect single-event transients. The paper describes an experiment in which transients were induced by a laser in a 90-nm CMOS device under test.

V. D. Agrawal (✉)
Department of ECE, Auburn University, 200 Broun Hall,
Auburn, AL 36849, USA
e-mail: vagrawal@eng.auburn.edu