Guest Editorial

Special Issue on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN)

Dimitris Gizopoulos • Said Hamdioui • Hans Manhaeve

Received: 18 March 2013 / Accepted: 18 March 2013 / Published online: 2 April 2013
© Springer Science+Business Media New York 2013

Electronic devices are pervading human lives in various areas and for a wide range of applications affecting our behavior; from medical to consumer electronics, from railways to the automotive and avionics scenarios and in server and cloud computing infrastructures. Reliability and dependable operation of such devices are critical issues and are pushing the requirement for dependable operation of computing systems for embedded as well as for high-performing applications way higher than ever in the past.

Constant research and development advances in manufacturing yield, lifetime and field reliability are important enabling factors to meet these requirements. But at the same time more challenges arise as both technology and architectures are at a turning point today. At the technology level many ideas are being proposed to push the end of Moore's law further ahead such as extending CMOS technology and deploying FinFET structures as well as finding alternatives to it like making use of carbon nanotubes (CNTFET), QCA, memristors, etc. From an architectural perspective, the spin towards deploying ever higher

frequencies and more aggressive dynamic instruction scheduling has been replaced by the trend of deploying a multitude of, usually simpler, cores on a single die.

These paradigm shifts in both manufacturing and architecture give rise to new dependability issues and require reflection and a rethinking of design, manufacturing, testing, and validation approaches suitable to the realization of reliable next-generation systems. The global understanding is that such manufacturability and dependability issues will only be resolved efficiently if industry and academia are jointly developing a cross-layer approach that takes technology, circuit and architectural aspects into account that can be deployed subsequently.

In the framework of the European Science Foundation (ESF) funded COST Action IC1103—MEDIAN (Manufacturable and Dependable Multicore Architectures at Nanoscale—<http://www.median-project.eu/>) and as an offspring of the MEDIAN 2012 inaugural workshop of this action that took place in conjunction with the 17th European Test Symposium 2012, we are glad to present this Special Issue in an archival journals in the field.

This Special JETTA Issue contains four papers covering a diverse set of topics related to manufacturability and dependability: from device level degradation and transient effects up to many-core architectural fault tolerance at high levels including software layers.

In the first paper, “On the simulation of HCI-induced variations of IC timings at high level”, by O. Heron, C. Bertolini, C. Sandionigi, N. Ventroux, and F. Marc, the authors deal with one of the most important circuit degradation mechanisms—the hot carrier injection (HCI), and propose a simulation and analysis framework at high level. In the second paper, “CEP: Correlated Error Propagation for Hierarchical Soft Error Analysis”, by L. Chen, M. Ebrahimi, and M. Tahoori, the authors analyze another important aspect of circuit reliability—the relation between low-level

D. Gizopoulos (✉)
Department of Informatics & Telecommunications,
University of Athens, Panepistimiopolis, Ilissia,
15784 Athens, Greece
e-mail: dgizop@di.uoa.gr

S. Hamdioui
Computer Engineering Laboratory,
Delft University of Technology, Mekelweg 4,
2628CD Delft, the Netherlands
e-mail: S.Hamdioui@tudelft.nl

H. Manhaeve
Ridgetop Europe, Lieven Bauwensstraat 20,
8200 Brugge, Belgium
e-mail: hans.manhaeve@ridgetop.eu

single or multiple transients and bit flips at logic or higher levels using fast estimation of error probabilities. The third paper, “Self-Adaptive Fault Tolerance in Multi-/Many-Core Systems”, by C. Bolchini, M. Carminati, and A. Miele, proposes a high-level, adaptive fault tolerant architecture for multi-core systems based on thread replication and re-execution. Finally, the fourth paper, “Reliability-Aware Heterogeneous 3D Chip Multiprocessor Design”, by I. Akturk and O. Ozturk, discusses a data/application mapping and processor layout approach for 3D chip multiprocessors

(CMPs) that maximize reliability of the final chip design without compromising performance.

We sincerely thank all European researchers involved in the MEDIAN action for their vivid participation and the European Science Foundation for supporting this valuable networking and research activity. We appreciate the time and effort that all authors of submitted papers and the reviewers allocated to this special issue.

We hope you will enjoy the MEDIAN Special Issue of JETTA.