Editorial

Vishwani D. Agrawal

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This issue contains ten papers and two *letters*. The topics covered are mixed-signal and RF testing (2 papers), modeling for process and environmental variations (1), verification (3), nonlinear circuits (1), fault simulation and untestable faults (2), and testing of 3D stacked ICs (1).

The third and fourth papers of this issue were originally presented at the *IEEE Latin-American Test Workshop (LATW)* of 2011. Victor Champac and Leticia Maria Bolzani Poehls (*JETTA* Guest Editor) were responsible for editing the versions appearing here. Five other papers as I have pointed out below have appeared in the *European Test Symposium (ETS)*. Their enhanced and revised versions were edited by Cecilia Metra.

Mixed-signal and RF testing is featured in the first three papers. The first paper is authored by Sheng and Kerkhoff from University of Twente, Enschede, The Netherlands, and Zjajo and Gronthoud of NXP Semiconductors, Eindhoven, The Netherlands. They provide an enhancement for specification-based test of an analog-to-digital converter (ADC). A signature generated by a pulsed input quickly identifies excessive parameter variation. The authors first presented this work in 2009 at the *ETS*.

Authors of the second paper are Sen, Banerjee, Natarajan, Devarakond, Choi and Chatterjee from Georgia Institute of Technology, Atlanta, Georgia, USA. From a single observation using an amplitude-modulated test stimulus they compute RF specifications such as gain, IIP2, IIP3 and P1dB.

The third paper deals with timing effects of variations in process, supply voltage and temperature. A delay model combining multiple variations is shown to work for 32 nm technology. This work is reported by Freijedo and Rodriguez-Andina

from University of Vigo, Vigo, Spain, Semião from University of Algarve, Faro, Portugal, Vargas from Catholic University – PUCRS, Porto Alegre, Brazil, and I. C. Teixeira and J. P. Teixeira from Technical University of Lisbon/INESC-ID, Lisbon, Portugal. They first presented it in 2011 at *LATW*.

Next, we have three papers on the theme of verification. The first of these proposes the use of mutations in a transaction level model (TLM) for fault injection at the register transfer level (RTL). TLM, which includes both software and hardware, is employed for system verification. Reusing faults (mutations) in TLM for hardware verification at RTL is shown to be an effective method. This work first appeared in 2011 at *LATW* and is reported by Guarnieri, Di Guglielmo, Bombieri, Pravadelli and Fummi from Università di Verona, Verona, Italy, and Hantson, Raik, Jenihhin and Ubar from Tallinn University, Tallinn, Estonia.

In the second paper on verification, the authors observe a lack of correlation between the results of simulation and formal property verification (FPV). Thus motivated, they define simplified assertions called test points whose coverage can be obtained by simulation as well as by FPV. The paper is authored by Hazra, Ghosh, Dasgupta and Chakrabarti from Indian Institute of Technology, Kharagpur, India.

The third paper on verification models applications of a system at the instruction level using data and control flow graphs. To model transient errors, some edges in their graph represent conditional dependencies subject to certain conditions in instructions. Assertion checking can then examine the behavior of the system in the presence of soft errors. The paper is authored by Izosimov from Semcon AB, Di Guglielmo, Lora, Pravadelli and Fummi from University of Verona, Peng from Linköping University, and Fujita from University of Tokyo. This work was first presented in 2011 at *ETS*.

Next paper provides a method for diagnosing multiple soft faults in nonlinear analog circuits. A soft fault, not to be

V. D. Agrawal (✉)
Auburn University,
Auburn, AL 36849, USA
e-mail: vagrawal@eng.auburn.edu

confused with soft error, is an analog fault such as an out of range parameter. A homotopy solution is shown to work better than the commonly used gradient methods. The authors are Tadeusiewicz and Hałgas from Technical University of Lodz, Lodz, Poland.

Three papers appearing next are derived from the program of *ETS* 2011. The paper by Bombieri, Fummi and Guarnieri of University of Verona in Italy provides a method to speed up fault simulation by RTL-to-TLM abstraction. The paper by Viilukas, Karputkin, Raik, Jenihhin and Ubar from Tallinn University of Technology, Tallinn, Estonia, and Fujiwara from Osaka Gakuin University, Osaka, Japan gives a method to identify untestable faults in the RTL description of a sequential circuit.

Taouil and Hamdioui of Delft University of Technology, Delft, The Netherlands, in their paper, propose the use of redundancy and repair for improving the yield of 3D stacked memories.

Of the two *JETTA Letters*, the first, authored by Ahmed, Wang and Ullah from Nanjing University of Aeronautics & Astronautics, Nanjing, China, and Ahmed from Institute of Space Technology, Pakistan, proposes the use of a multi attitude decision making (MADM) procedure for diagnosing faults in analog circuits. In the second *letter*, Sindia and Agrawal from Auburn University, Auburn, Alabama, USA, and Singh from Indian Institute of Technology Bombay, Mumbai, India evaluate the defect level of an analog circuit tested by a previously proposed polynomial coefficient method.