Editorial

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This issue contains ten papers. The topics covered are analog and mixed-signal test, random testing, memory test, noise and reliability issues, automatic test equipment, and delay testing. All three papers on noise and reliability issues were originally presented at the *IEEE Latin-American Test Workshop (LATW)* of 2011. Fabian Vargas was responsible for the editing of these papers as they appear here.

Analog and mixed-signal test is featured in the first three papers. In the first paper, Ting of National Kaohsiung University of Applied Sciences, Kaohsiung, Taiwan, proposes an alternate test for operational amplifiers. The device under test (DUT) is configured as a unity gain amplifier supplied with a digital clock input. The input and output of DUT are passed through an exclusive-OR gate and then processed by a digital counter such that the count must match a specified value that characterizes the fault-free DUT.

In the second analog test article, authors, Luo, Wang and Lin of Nanjing University of Aeronautics and Astronautics, Nanjing, China and Jiang from Anhui University of Science and Technology, Huainan, China, discuss fault dictionary based diagnosis. They provide a method for selecting measurement nodes to reduce the ambiguity in the test result.

The following paper, also on analog circuit diagnosis, is authored by Long, Tian and Wang from University of Electronic Science and Technology of China, Chengdu, China. The authors use a support vector machine (SVM) to diagnose circuits with component tolerances. Their SVM has a least squared term added to the cost function. The paper claims to achieve greater efficiency than the alternative techniques that rely on neural networks.

Next, Mrozek and Yarmolik from Bialystok University of Technology, Bialystok, Poland, discuss a method for generating random inputs for digital test. They use the concept of antirandomness where the idea is to avoid clustering in the sample space. Random vectors are iteratively generated using an MMHD (maximal minimal hamming distance) metric. The results show greater fault coverage efficiency compared to other forms of random tests.

The next article analyzes resistive bridging defects of SRAM devices. Error sensitivity to bridging defects is shown to increase as technology advances through 90 nm, 65 nm and 40 nm. It is shown that a weak read is the most likely error caused by bridging. The paper is authored by Fonseca, Dilillo, Bosio, Girard, Pravossoudovitch and Virazel of LIRMM, University of Montpellier, France, and Badereddine from Intel Mobile Communications, Sophia-Antipolis, France.

The next article, first of three on noise and reliability issues, is authored by Castellani-Coulié, Aziza, Micolau and Portal from Université Aix-Marseille in France. From the simulation of a three-dimensional model of a 90 nm SRAM cell, the authors develop an RC circuit model that mimics the single event upset (SEU) of the memory cell.

The following article proposes the use of an on-chip voltage sensor to detect radio frequency interference on test chips. The test chips then allow noise immunity assessment of a design before production. The authors are Ben Dhia and Boyer of Université de Toulouse, France, and Vignon and Deobarro from Freescale Semiconductor, Toulouse, France.

Next, follows an article, authored by Ferri, Papagiannopoulou and Bahar of Brown University, Providence, Rhode Island, USA and Calimera from Politecnico di Torino, Torino, Italy, that proposes a software technique to alleviate the aging effect of NBTI (negative bias temperature instability)

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in scratchpad memory devices. The main idea is to spread around the available idleness among memory sub-banks.

The next paper discusses test challenges of electronic devices that are related to cost, time-to-market and quality. The authors, Vock, Escalona, Turner and Owens from University of Ulster, Nanotechnology and Advanced Materials Research Institute, Antrim, United Kingdom, emphasize the use of open-source test programming software and a test expert system. Their study outlines the capabilities of the Eclipse system.

The final article is on delay testing and is authored by Yi of Kwangwoon University, Republic of Korea and Hayes from University of Michigan, Ann Arbor, Michigan, USA. The authors study high-level robust coupling delay tests. Being implementation-independent, these tests are long. They use a partial order relationship among the tests for minimization, preserving the robustness of path delay testing. Although an average test set reduction of 35 % is observed, the authors report above 80 % reduction when the circuit function is unate.