Editorial

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This issue of *JETTA* contains twelve papers. The topics covered are ATE, mixed-signal test, RF test, BIST, functional verification, fault-tolerant systems, maintenance test and test data compression. The first paper is derived from the *IEEE European Test Symposium (ETS)* of 2009. Five other papers in this issue had their initial presentations made at the *IEEE Latin-American Test Workshop (LATW)* of 2010. Cecilia Metra (ETS) and Fabian Vargas (LATW) conducted the journal's peer review procedure for respective papers. We thank them for their work.

In the first paper the authors, Han, Park, Lee, Chung, Byun, Woo, Oh and Abraham from University of Texas, Austin, USA, provide a method for measuring and compensating for time skew of signals using the time domain reflectometry. The technique emphasizes large dynamic range and fine grain resolution. Authors first presented this work at ETS in 2009.

The second and third papers discuss mixed-signal test. The paper by X.-L. Huang of Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, and Kang, Yu and J.-L. Huang of National Taiwan University, Taipei, Taiwan, describes histogram-based testing of ADCs. This technique assesses the amount of non-linearity and then restores linearity with a focus on reducing the hardware needed for doing so. Another paper by Ting of National Kaohsiung University of Applied Sciences, Kaohsiung, Taiwan, gives a design for output response analyzer (ORA) hardware in a BIST system for ADCs. The ORA is implemented as a digital circuit, which is independently testable.

The fourth article discusses radio frequency (RF) test. Radhakrishnan and Ozev of Arizona State University, Tempe, Arizona, develop a sampling method to compute thresholds to classify the test response as fault-free or faulty. Although the sampling method uses Monte Carlo simulation, it is much less complex than the conventional Monte Carlo simulation.

The fifth article deals with built-in self-test. The paper by Sun of Zhengzhou University, China, and Zeng, Li, Lei and Shao of Xi'an Jiao Tong University, China, describes a novel method for generating test patterns. A coverage driven algorithm generates seeds, which then drive the generation of single input change (SIC) patterns. The authors report higher coverage with shorter test length while the SIC patterns reduce test power.

The sixth and seventh papers, both presented at LATW 2010, discuss functional verification. Márquez, Tobar, Strum and Chau of University of Sao Paulo, Brazil, present a simulation based verification procedure using constrained random input patterns. The next paper is authored by Grosso, Ravotto, Sanchez, Reorda and Tonda of Politecnico di Torino, Italy, and Holguin and Medina of Universidad del Valle Cali, Colombia. They generate input stimuli to completely cover all functions. Patterns are generated by a testbench and application to a direct memory access (DMA) controller is discussed.

The next three papers are on fault-tolerant systems. A paper by Bahramali, Jiang and Reyhani-Masoleh of University of Western Ontario, London, Ontario, Canada, proposes a time-redundancy based fault diagnosis scheme for hardware implementing the secure hash algorithms (SHA) used in security protocols. The next paper, authored by Munaretti, Weber, Cechin and Fiss of Federal University of Rio Grande do Sul, Porto Alegre, RS, Brazil, examines

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the fault injection methods for indentifying and recreating faults in electronic systems. Another paper by Azambuja, Pagliarini, Rosa and Kastensmidt of Federal University of Rio Grande do Sul, Porto Alegre, RS, Brazil, analyzes software techniques to combat faults of an electronic system caused by single event upset (SEU) in memories and single event transient (SET) in combinational logic. The last two papers of this group were first presented at LATW 2010.

The eleventh paper in this issue is authored by Gonçalves, Balen, Lubaszewski, Schneider, Henriques and Bosa of Federal University of Rio Grande do Sul, Porto

Alegre, RS, Brazil. They discuss a system maintenance scheme in which neural networks or self organizing maps are used to detect, diagnose and predict faults in an electronically controlled system. This paper was also previously presented at LATW 2010.

The final article is authored by Zhang, Kuang and You of Hunan University, Changsha, China. Their method of test data compression partitions test sets into four types of blocks, namely, all-0 blocks, all-1 blocks, sparse blocks with very few specified bits and characterless blocks. Suitable encoding then results in test data compression and allows decoding of the compressed data.